FABRICATION AND RELIABILITY TESTING OF COPPER-FILLED THROUGH-SILICON VIAS FOR THREE-DIMENSIONAL CHIP STACKING APPLICATIONS

by

ALPHONSE MARIE KAMTO TEGUEU

A DISSERTATION

Submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering in the Graduate School of The University of Alabama

TUSCALOOSA, ALABAMA

2010
ABSTRACT

Through-silicon vias (TSVs) have been extensively studied because of their ability to achieve chip stacking for enhanced system performance. The fabrication process is becoming somewhat mature. However, reliability issues need to be addressed in order for an eventual transition from laboratory to production. This dissertation discusses the TSV fabrication process, testing results for TSV reliability investigation of an integration of TSVs and capacitor devices.

In our laboratory, vias with tapered sidewalls are formed through a modified Bosch process using deep reactive ion etching (DRIE). Cryogenic etching is also considered as a means to etch vias without sidewall scalloping that is observed for the Bosch process. Vias are lined with silicon dioxide using plasma enhanced chemical vapor deposition (PECVD) followed by a sputter deposited titanium barrier and a copper seed layer before filling by a reverse pulse copper electroplating process. Following attachment of the process wafer to a carrier wafer, the process wafer is thinned from the backside by a combination of mechanical methods and reactive ion etching (RIE). Fabricated vias are subjected to thermal cycling with temperatures ranging from -25 °C to 125 °C. TSVs are shown to be stable with small increases in measured resistance for 200 cycles. In addition, small changes in resistance are observed when vias are held at elevated temperatures for extended periods of time.

Integration of decoupling capacitors with TSVs represents a good alternative to conventional 2-D layouts to achieve miniaturization and increased density. Therefore, decoupling capacitors can be brought in close proximity to the active elements, thereby, reducing
their parasitic inductance and allowing higher clock rates. In this study, capacitors with anodized tantalum as the dielectric are integrated with TSVs without negatively impacting their operation. The performance of these capacitors was evaluated by measuring resonant frequency, parasitic inductance, and parasitic resistance.
DEDICATION

To my lovely wife, Dr. Yolande Konguep Tchouangue.

To my late parents Marie Madeleine and Emmanuel Tegueu.

To all my brothers and sisters.
ACKNOWLEDGMENTS

I would like to express my profound gratitude to my advisor, Dr. Susan L. Burkett, whose expertise, understanding through the duration of this dissertation, added considerably to my graduate experience. Her guidance and support helped me succeed and made the Ph.D. journey more enjoyable. The author would like to thank her for the opportunity given to work with the project supported by Air Force Research Laboratory (AFRL) under Grant FA8650-04-2-1619. I am also grateful to the members of my committee, Dr. Sushma Kotru, Dr. Seongsin M. Kim, Dr. Shuhui Li, and Dr. Gregory B. Thompson for their inputs and interests in this research.

This research was possible through the use of the High Density Electronic Center facility at the University of Arkansas. Sincere thanks to Errol Porter, Michael Glover, Jeff Mincy, and Mike Steger. Likewise, collaboration and help received from Dr. Anirhuda Sumant and Dr. Ralu Divan at Argonne National Laboratory is deeply appreciated. I had a marvelous research group and I thank Dr. Isibhakhomen Abhulimen, Dr. Yang Liu, Dr. Susan Jacob, Madhav Rao, Trang Lam, and Gayathri Jampana for all the challenging times we had in the clean room and outside.

Sincere thanks to my friends Dr. Roger Nana and family, Mr. Blanchard Kenfack and family, Mr. Francois Kuate, Mr. Remond Mbiada, Mr. Randy Nix and family, Mr. Joseph Kuate and family, and Ms. Shanique Murray for their advice throughout the Ph.D. journey.

Special thanks to my beloved wife Yolande for her support and encouragements. I am most thankful to my parents, all my brothers and sisters for their help and constant support in challenging times. I know I can always count on you all.
To God the almighty for all his blessings

This research was supported by Air Force Research Laboratory (AFRL) under Grant FA8650-04-2-1619, and by the College of Engineering at The University of Alabama.
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CHAPTER 1

INTRODUCTION

1.1. General Introduction

A through-silicon via (TSV) is a vertical electrical connection (via) passing completely through a silicon wafer or die. Metal filled TSVs allow devices to be connected using a three-dimensional (3-D) approach. Optimizing and refining this technology has been a focus for the semiconductor industry the past few years because of the need for novel integrated circuit (IC) packages that can address the issues associated with increased functionality and performance while reducing size and costs for a growing number of defense and consumer electronic applications [1-3]. This technology could be adopted for many applications in the future because of the capability in solving problems related to electrical performance, memory latency, power and noise on-and off-chip. An application of TSVs in production today involves CMOS image sensors where the active silicon area is bonded onto glass and contacted from the backside [4-7]. In a recent issue of Semiconductor International, both Samsung and Elpida have outlined plans for production of 8 Gigabit DRAM with 3-D TSVs [8]. TSVs used in stacked chip applications are an enabling technology for integration of complex systems [9-13].

A variety of materials and deposition methods have been proposed and tested for TSV applications. Feature dimensions, final material deposit characteristics, and process reliability [14] are some of the main limiting factors to the application of these materials and methods along with typical cost considerations [1]. Copper is the most common conductive material used to fill vias because of its low electrical resistance, compatibility to conventional multilayer interconnections, and the relatively good match to silicon’s
coefficient of thermal expansion. Because it is difficult to fill high aspect ratio vias without introducing voids through conventional damascene electroplating, several approaches involving electrodeposition have been developed. The deposition approaches typically involve optimization of the electroplating bath, use of a reverse pulse waveform, and regulating the current density [15-17]. TSV interconnects have been the focus of many researchers worldwide because of the potential for reducing signal delay, feature size, and power consumption by allowing structures from different planes to be brought close together. Proven density and compact form are the main factors driving TSVs for 3D interconnects. Wire bonding is limited in density and performance, flip chip in stacking. Allowing stacking, density and enhanced performance, TSVs are suitable for further scaling efforts within the semiconductor industry.

1.2. Dissertation Motivation and Goal

Fabrication of reliable vias is a requirement in accomplishing TSV chip integration. Much of the published work on TSVs involves the processing and integration issues with only a small amount of attention given to modeling, characterization, and reliability testing. Via etching, lining, and filling play a crucial part in the TSV process flow. Part of the work described in this dissertation focuses on the variety of via profiles that can be obtained by varying etch process parameters. In one study, inductively coupled plasma (ICP) cryogenic etching is investigated as a way to etch vias without the scalloping along via sidewalls as observed when using deep reactive ion etch (DRIE), or the Bosch process, routinely used in fabricating microelectromechanical systems (MEMS). ICP cryogenic etching represents an alternative to Bosch etching with one advantage being higher silicon etch rates.
The overall goal of this research project is to fabricate robust TSVs that are compatible with CMOS process technology. Demonstrating the integration of TSVs with electronic devices without negatively affecting their operation represents another area of study. In this work, capacitors with tantalum oxide dielectric are integrated with TSVs.

1.3. **TSV fabrication Process Flow**

The process flow used to fabricate TSVs is shown in Figure 1.1.

![Image of TSV fabrication process flow](image)

1. Via etch  
2. Via lining  
3. Via filling  
4. Front side patterning  
5. Wafer attachment  
6. Wafer thinning  
7. Selective silicon etch  
8. Insulation deposition  
9. Via exposure  
10. Barrier/seed deposition  
11. Pattern pad plating  
12. Pattern seed/barrier etch

Figure 1.1. Process flow for the fabrication of TSVs.
The fabrication of TSVs includes the following major steps: formation of blind vias; via lining and filling; attachment of process wafer to a carrier wafer; backside thinning; wafer backside processing. Once complete, samples are tested for reliability. Key processes during this study are discussed in the following sections.

1.3.1. Formation of blind vias

Conventional reactive ion etching (RIE) techniques can be used to etch vias in a Si substrate. This process yields vias with a tapered sidewall due to the isotropic nature of the etch. This type of profile, a larger opening at the top of the via, allows higher conformality for films deposited after the etch using processes such as plasma enhanced chemical vapor deposition (PECVD) and sputtering techniques. This sidewall taper is required when lining vias beyond a critical aspect ratio and constrained by these deposition techniques. RIE is a dry etching technique in which a plasma is formed by chemically reactive gases. Reactive species are accelerated toward the surface where they remove any unprotected material. A capacitively coupled electrode system is used in RIE with reactive gases brought together inside the chamber. An RF (13.56 MHz) system generates a plasma of positive ions. The ions are accelerated toward the wafer (negative electrode) where the reaction occurs. Sulfur hexafluoride (SF$_6$) and tetrafluoromethane (CF$_4$) are commonly used for fluorine-based etching of silicon. Higher etch rates are obtained using SF$_6$. Addition of O$_2$ to these gases helps to control etch rate and selectivity. The main drawback in using this process for via etch is the poor selectivity between silicon and the masking material. For this reason RIE is typically used to etch only relatively shallow vias. When creating deep vias in silicon, alternative etch techniques are used. For most of the reported work, an STS deep reactive ion etch
(DRIE) tool is used. This process exhibits very good selectivity between silicon and the masking material. Because of the high selectivity, photoresist can be used as the masking material. DRIE is a popular technique for etching silicon and is commonly used in the microelectromechanical systems (MEMS) area. A common method for etching silicon is the Bosch process, a patented process [18] that alternates etch and passivation cycles. In the etch cycle, SF$_6$ is chosen for its ability to release fluorine atoms to etch silicon through generation of volatile SiF$_4$. The fluorocarbon C$_4$F$_8$ is the passivation gas and is used to create a polymer coating that has a protective effect on the via sidewall. The Bosch process is designed to create vias with vertical sidewalls by repeated etch and passivation steps. A cross section at the beginning of a silicon etch is shown in Figure 1.2.

![Diagram of Bosch process](image)

**Figure 1.2.** Basic steps in the Bosch process [19].

To create a tapered sidewall for ease in depositing materials that completely line the via, the Bosch process recipe can be modified. The modification comes from adjusting passivation cycle times in order to change the amount of passivation material that is available to protect the sidewalls throughout the etch cycle. A study of the effect of
process parameters on the via profile is given in [20]. One important parameter that can be controlled is the scalloping that results from the alternating nature of this etch. Scallop size has been shown to increase with coil power and is illustrated in Figure 1.3 [20].

![SEM cross sectional views of a via showing the effect of varying the coil power on via sidewall scallop size](image)

Coil power = 300 W  
Coil power = 200 W

**Figure 1.3.** SEM cross sectional views of a via showing the effect of varying the coil power on via sidewall scallop size [20].

### 1.3.2. Deposition of insulation, barrier, and seed layers

A silicon dioxide (SiO₂) layer, 2 µm in thickness, is deposited at 250 °C using a PECVD system and SiH₄ and O₂ gases. This provides the via insulation layer. Sputtering titanium (0.5 µm) to serve as a barrier layer is performed at a pressure of 5 mTorr and a power of 2500 W. This is followed by sputtering a copper seed layer (2 µm) at the same pressure and a power setting of 3000 W. The sputtering process begins with a 60 sec RF etch to clean the wafer surface. Insulation, barrier, and seed layers lining the via need to be as conformal as possible for appropriate coverage as illustrated in Figure 1.4 [21].
1.3.3. **Via filling**

Copper can be deposited through a variety of techniques such as chemical vapor deposition (CVD) or physical vapor deposition (PVD). However, the most common technique for depositing copper into trenches and vias is by electroplating [22]. CVD applications typically involve the use of unstable and hazardous organo-metallics which result in deposits with lower purity and higher resistivity. Electroplating is preferred for its speed, stability, ease of control and maintainability [22, 23]. Electroplating processes are typically performed at room temperature and pressure, so the equipment is less complex and less expensive than vacuum deposition equipment. Hence, the majority of TSV development work focuses on the use of electroplating. Being well known as a process for copper damascene interconnects, it is believed that technology transfer will be easily adopted by the semiconductor community. Via filling is a complex process and electroplating performance varies with several plating parameters. In order to further increase throughput, continuous efforts to develop faster and more stable processes are in progress [22].
Different factors affect the via filling process including increased transport of the solution at the top of the via and a higher field at the small curvature leading to a fast build-up of deposited material at the via opening. These factors may lead to a possible pinch-off of the via before complete filling introducing voids in the deposited material [24]. To achieve a bottom-up filling without voids, deposition at the surface needs to be reduced at the same time it is accelerated at the base. For this purpose, the composition of the copper electrolyte plays a significant role in achieving good process performance. There are three organic additives designated as accelerators (or brighteners) that accelerate plating inside the via, suppressors (or carriers) that reduce plating rate at the via mouth, and levelers that substantially enhance copper planarity across the wafer surface. These organic additives are used with the appropriate plating chemistries in addition to the inorganic components of metallic ions, acid (sulfuric or methane sulfonic based), and halide ions such as chloride. Other requirements for achieving void-free filling are good wettability (especially when smaller vias with high aspect ratio are involved), and stability for larger features that require longer processing times. If an oxide layer is present at the seed layer’s surface, an etching step using dilute acid solution is required. Beyond high performance chemicals, successful processing of TSV structures also requires a good wafer design (via profile and smoothness), seed layer continuity, and high performance equipment. In particular, periodic reverse pulse plating improves mass transport conditions inside the via through adsorption/desorption phenomena which are not possible otherwise [25]. A cross sectional image of a filled tapered blind via is shown in Figure 1.5.
Different via profiles were investigated for lining and filling processes [26]. Optimizing the plating process helps to achieve void-free filling. Our approach to this optimization includes: use of a fountain plating system that provides agitation and allows the plating solution to reach the base of the vias; control of organic additives; and use of appropriate current density levels.

1.4. **Overview of Heterogeneous Integration**

Key advantages of TSV technology include shorter connections with significant reduction of information flow on a chip (by up to 1000 times) [27]. TSV connections also allow the addition of increased number of channels or pathways (up to 100 times more than 2-D chips) [27]. TSVs can replace less efficient wire bonds for transferring signals off the chip. They also increase speed while reducing power consumption up to 20% through uniform power delivery to all parts of the chip [27]. The energy dissipated in an electronic system is given by: \( E = CV^2 \) and the power consumed is given by \( P = fCV^2 \),
where \( V \) is the voltage across the capacitance \((C)\) and \( f \) is the frequency. The capacitance is proportional to the interconnect length and according to these equations, the total power consumption is reduced directly in proportion to the overall reduced parasitic values.

Our research group has been working on an integrated process flow for the fabrication of TSVs, electrical testing for reliability of the vias, development of copper post plating used in chip assembly, and a thermal management scheme leading to a demonstration vehicle as shown in Figure 1.6.

![Schematic of the overall heterogeneous system integration concept](image)

**Figure 1.6.** Schematic of the overall heterogeneous system integration concept [10].

Different assembly schemes are used for chip stacking including wafer level and chip level bonding even though copper posts are increasingly used instead of solder balls due to their compliance [28] and reduced pitch capability. Increased density comes with increased heat generation. For our integration scheme, Si and GaAs electronic layers are to be connected using TSVs along with an array of posts contained by a dam structure [10]. Copper posts provide compliance between the dissimilar electronic materials and
also allow coolant fluid to flow in between. The area between chips can also be used for integrated decoupling and power distribution as shown in Figure 1.6. Yield of the system can be improved through this scheme by testing individual die before assembly.

A copper-tin intermetallic compound is used to bond the copper posts to TSVs. The copper posts are approximately 35 µm in diameter and 100 µm in height. They are fabricated by DC electroplating at a current density of 20 mA/cm² for 5.5 hrs into a deep mold formed by KMPR negative resist. Because the posts are not uniform in height along the wafer, a polishing step is introduced to level their height within the mold. A 3 µm tin layer is plated to cap the top of the copper posts by DC electroplating following another patterning step using the same photomask. This process forms a Cu₃Sn intermetallic compound that behaves in a similar way to soldering by way of a solid-liquid interdiffusion process [29, 30]. The compound forms at 300 °C but will not remelt below 600 °C. Initial electroplating of tin was found to yield a grainy structure, but reducing the current density from 20 to 3 mA/cm² results in a smooth, fine grain structure. SU-8 photoresist was initially used to create the mold on a sputtered Ti/Cu layer although removal of resist residue on the copper posts was a challenge. For this reason SU-8 was replaced by the KMPR 1000 series resists supplied by MicroChem Corporation for creating the mold. KMPR resist is easy to remove and is dual spin coated at 2800 rpm each time to achieve a 100 µm thick resist film. The wafer is baked at 100 °C for 5 min and cooled before applying the second layer. The wafer has a second soft bake for 18 min at the same temperature. A post exposure bake is carried out at 105 °C for 4 min. A SEM image of copper posts created using this procedure is shown in Figure 1.8.
Figure 1.7. SEM image of copper posts capped with tin.

1.5. **Dissertation Organization**

The remainder of the dissertation describes key findings. Chapter 2 discusses cryogenic etching as a way of fabricating vias with a tapered via sidewall and an elimination of the scalloping that results from the Bosch process. Chapter 3 provides insights on thermal cycle testing of TSVs that previous DC tests show to be high in yield and electrically reliable. Chapter 4 discusses the integration of capacitors using Ta$_2$O$_5$ dielectric with TSVs. Chapter 5 presents the summary and comments about future work. The appendices provide process travelers as well as other information relevant to completing this research.

1.6. **Chapter 1 References**


CHAPTER 2
CRYOGENIC INDUCTIVELY COUPLED PLASMA ETCHING FOR
FABRICATION OF TAPERED THROUGH-SILICON VIAS*

Abstract

Vertical interconnects pose an interesting method for heterogeneous integration of electronic technologies allowing three-dimensional (3D) stacking of MEMS devices and IC components. The vertical interconnects, referred to as through-silicon vias (TSVs), begin with formation of blind vias in silicon that are eventually exposed by mechanically lapping and polishing the wafer backside. Inductively coupled plasma (ICP) etching using SF$_6$/O$_2$ gas chemistry at cryogenic temperatures has been investigated as a way to form vias with a tapered sidewall. The point in creating a controlled taper is so that subsequent thin films can be deposited along the sloped sidewall that line the via with insulation, barrier, and seed films. This tapering is necessary if the via lining processes do not provide adequate conformal coverage, a common problem for conventional low temperature deposition processes. In our process for lining the via sidewall, plasma enhanced chemical vapor deposited (PECVD) silicon dioxide is used to insulate vias from the surrounding silicon. Both Ti and Cu are sputter deposited and provide protection from copper migration and a seed film for Cu electrodeposition, respectively.

After etching and lining, the vias are filled by reverse pulse plating of Cu. Vias are 20 - 25 μm in diameter and etched using different masking materials. The effect of changing gas flow rates, chamber pressure, ICP power, and substrate temperature on etch

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rate, via profile, and sidewall morphology will be presented. These parameters are critical in optimization of an etch process for vias of specific dimensions to be used in 3D integration.

2.1. Introduction

TSVs have been extensively studied because of their ability to achieve chip stacking leading to an overall enhanced system performance in a reduced amount of space. Extensive studies have been performed on via formation using deep reactive ion etching (DRIE) with a Bosch process, especially the effect of process parameters on via profile and sidewall roughness [1]. Unfortunately, this process yields scalloping along the via sidewall due to the nature of the process that involves a large number of alternating etch and passivation cycles. While the size of the sidewall scallops are on the nanometer scale, this morphology can prevent conformal deposition of the materials intended to line the via along the via sidewall and base. This is especially true if the via also possesses a straight sidewall. Sidewall angle is defined to be the supplement of the angle between the sidewall and base. Previous studies reveal a critical sidewall angle of 87 degrees [2] leads to conformal lining of materials inside the via and periodic pulse plating aids in achieving bottom-up via filling without internal voids [3] thereby improving reliability for TSVs [4].

Anisotropic profiles are achieved when forming via holes by balancing the amount of via sidewall passivation material with the bombardment of ions from the plasma that are directed toward the base of the via. Researchers primarily use two etch processes for this purpose. The first one, termed the Bosch Process [5], operates at room
temperature and achieves anisotropic etch profiles by successive cycling of SF₆ etch and C₃F₈ passivation gases using an inductively coupled plasma (ICP). This technique is extremely useful for etching deep vias and trenches and is commonly used by both 3D integration and MEMS communities [6-8].

The second method typically uses SF₆ and O₂ gases in an inductively coupled plasma for directional etching. Jansen et al. studied deep silicon and polymer trench etching with SF₆/O₂/CHF₃ to create various profiles where etch rate is optimized by controlling process parameters [9]. Etching at cryogenic temperatures was introduced by Tachi et al. [10]. Bartha et al. showed that at temperatures as low as -100 °C, etch selectivity greater than a value of 100 is achieved using a SiO₂ mask [11]. In this process, sidewall protection is achieved through formation of an SiOₓFᵧ inhibiting layer. It has been demonstrated that via profile can be dramatically changed from negative to positive taper by balancing the etching and deposition rates of this layer with respect to the removal of silicon [12, 13]. F-radicals isotropically and spontaneously etch silicon and are obtained from decomposition of SF₆. Other researchers have shown that oxygen radicals in the SF₆/O₂ plasma chemistry help to create the SiOₓFᵧ inhibiting layer [14]. By lowering the wafer temperature to cryogenic temperatures, the volatility of the SF₄ reaction product is reduced and passivation is enhanced [15]. Therefore, the etching process takes place only in the direction of ion bombardment resulting in higher anisotropy as the base sustains higher kinetic energy [16]. The passivation layer is removed from this area, silicon is exposed and etching follows.
2.2. Cryogenic ICP Etching

The main advantages of cryogenic etch processes compared to room temperature Bosch etch processes are higher etch rates, a single process step with smoother sidewalls (no scalloping), and elimination of chamber sidewall polymer contamination that requires chamber cleaning. Craciun et al. and Dussart et al., through XPS analysis, showed that negligible oxidation occurs during the process and that the passivating film is removed when the wafer is warmed to room temperature [17, 18].

Previous studies of cryogenic etching have produced various process recipes with the majority of those studies dedicated to etching trenches rather than via holes. All processes need to be optimized for the specific equipment under study and a particular application as the results are influenced by many factors including: aspect ratio of the feature; the size and shape of mask opening; pattern loading; and masking material. In our case, fabricating TSVs for the purpose of stacking silicon-based electronics with GaAs-based electronics is the application. The effect of variable chamber pressure, ICP power, gas flow rates, and substrate temperature on the via profile, etch rate, and sidewall morphology is the focus of this study. These aspects are critical in the optimization of an etch process recipe for vias of specific dimensions. Finally, the optimized via profile is used to show conformal lining of insulation, barrier and seed layers before filling by copper electroplating.

Process parameters have been studied for ICP etching of tapered via holes at positive temperatures. It has been shown that the amount of O$_2$ in the SF$_6$/O$_2$ gas mixture is one of the most important parameters for producing sidewall tapering and undercut formation [19,20]. Undercut refers to an increased lateral etch at the top of the via just
beneath the mask material. Likewise, spikes are generated and sidewall roughness occurs when the amount of \(O_2\) to \(SF_6\) increases even though increasing the temperature can alleviate this problem. Similar work has been performed at cryogenic temperatures and very useful guidelines have been developed [13] for etching a broad variety of MEMS structures using the black silicon method [9]. This method relies on the fact that silicon turns black when the vertical sidewall recipe is obtained to determine a good balance between etching and passivation [9]. Even though these guidelines focus on general trends, it is clear that profile control results from striking a balance between etching silicon and depositing \(SiO_xF_y\). The amount of passivation material is mainly determined by both substrate temperature and the \(O_2\) content in the gas mixture.

Both low temperature reactive ion etching and microwave plasma etching of silicon show a suppression in sidewall reactions by lowering the temperature in the range of \(-130\) to \(-100\) °C [10]. In the same study, the authors found that etching does not take place below \(-140\) °C as the \(SF_6\) gas starts to freeze on the cold surface. The etch rate at temperatures in the range of \(-130\) to \(-100\) °C is relatively low, in the range of 500 nm/min for micro-scale structures [10]. Improvements have been made in this area and cryogenic etching of via holes as deep as 400 μm exhibit etch rates as high as 7 μm/min [20]. The process is very sensitive to temperature variations [21]. In other studies that focus on developing processes for etching trenches with good profile control at cryogenic temperatures, it was found that decreasing chamber pressure yields high verticality because of an increased mean free path for reacting ions [16, 22]. The same vertical profile is observed when the rf forward power is increased due to increased ion energy. It has also been shown that by reducing substrate temperature, the amount of undercut can
be reduced although not totally eliminated [16, 22]. A study on the origin and control of undercut in deep plasma etching at cryogenic temperatures indicates that undercut is caused by reaction of F-radicals on the sidewall and can be minimized through a highly anisotropic process with the substrate temperature set to approximately -100 °C [23]. At this temperature, the reaction probability of fluorine radicals on the sidewall decreases while the sticking coefficient of the passivating precursor increases. From published work, there is potential for achieving an etch rate of 5 μm/min for 2 μm wide trenches [14].

2.3. Etch Mask Materials

Finally, the effect of masking material in cryogenic etching also has to be considered. Negative resists, such as SU-8, at thicknesses as high as 60 μm are suitable for cryogenic processing without exhibiting cracks [24]. Experimental results suggest the resistance to cracking is due to exceptionally high cross-linking density observed in SU-8 resists. Positive resists require a thin layer to avoid cracking and so are used only when shallow etching is needed because of poor selectivity. Two mechanisms including thermal expansion mismatch and mechanical wafer deformation induced by the helium backside cooling system were demonstrated to play an important role in the cracking process [24]. Hence, hard masks are more robust in deep etching at cryogenic temperatures with SiO₂ being one of the most common reliable mask materials. This mask material has moderate selectivity compared to an Al mask although is preferred in through-wafer etching because Al exhibits a micromasking phenomenon. Likewise, Al has been shown to be an inappropriate material for clamping rings as it becomes
polarized in an active plasma because of its high conductivity. Self sputtering leads to local transfer of small amounts of Al atoms on the wafer causing a micromasking of silicon that affects the etch process [25]. An insulating ceramic clamping ring has been proposed as a replacement for Al to prevent formation of what is commonly referred to as silicon grass, the formation of vertical needle-like silicon structures due to this micromasking effect.

2.4. Experimental Procedures

A Plasmalab System 100 etch reactor made by Oxford Instruments is used to conduct plasma etching experiments at cryogenic temperatures. This system contains two power sources capable of generating a high density plasma from a SF$_6$/O$_2$ gas mixture injected in the inductively coupled plasma (ICP) source. The gas mixture flows into the chamber by way of calibrated mass flow controllers. The second power source is a capacitively coupled plasma (CCP), or rf source, which independently accelerates and controls both ion flux and energy from the plasma toward the wafer surface. Hence, both flux of radicals and ionic species from the SF$_6$ plasma are independently controlled by these power sources operating at 13.56 MHz.

The silicon wafers are mechanically clamped to a liquid nitrogen cooled substrate electrode. Helium is circulated on the wafer back side to ensure effective heat exchange and temperature control between the liquid nitrogen cooled electrode and the wafer. A high conductance pumping system also allows high gas flows of SF$_6$ at relatively low operating pressures to achieve a high etch rate. The process parameters in this study are varied using the following ranges:
• pressure (8-20 mTorr),
• temperature (-130 to -80 °C),
• ICP power (500-1,000 W),
• SF\textsubscript{6} flow rate (30-36 sccm), and
• O\textsubscript{2} flow rate (3-6 sccm).

All parameters are varied in small ranges near, what we refer to as, the baseline recipe. This process baseline recipe was determined by preliminary experiments where parameters were varied until a small amount of sidewall tapering and sufficiently high etch rates were achieved. The values in the baseline recipe include: a pressure of 12 mTorr; a temperature of -100 °C; an ICP power setting of 700 W; a rf power setting of 3 W; 36 sccm SF\textsubscript{6} gas flow; and 4 sccm O\textsubscript{2} gas flow. These baseline values are also similar to the manufacturer recommended values for this system (10 mTorr, -110 °C, 700 W (ICP), 3 W (rf), 40 sccm SF\textsubscript{6}, and 6 sccm O\textsubscript{2}).

Commercially available n-type phosphorous-doped wafers are used with specifications: 100 μm diameter 525 ± 25 μm thick, 1-10 Ω-cm resistivity, and <100> crystal orientation. Various masking materials have been investigated including 1 μm silicon dioxide, thermally grown by steam oxidation, sputter deposited chromium (40 nm) and aluminum (200 nm), and three positive photoresists (PR S1813, SPR220-3, and PR S1827). Wafers are spin coated with PR S1813 for 30 sec at 3000 rpm following application of an adhesion promoter (HMDS) at 150 °C. Wafers are soft baked at 110 °C for 90 sec, exposed and developed using Microposit 351 aqueous alkaline solution (3:1 deionized water:developer). In the case of thermally grown oxides, a buffered oxide etch
(BOE) solution is used to etch the patterned oxide. Chromium and aluminum etchant solutions are used for those particular masks.

The photomask used in this study has circular openings of both 20 and 25 μm diameters, which increases by 2 μm for each via hole following the patterning step. Finally, the pattern loading was a value of 3 %. Following the etch process, wafers are cleaved and the cross-sections are examined using a FIB FEI NOVA 600 system.

2.5. Results and Discussion

In the following sections, the effect of substrate temperature, percentage of oxygen in the gas mixture, chamber pressure, ICP power, and masking material on etch rate, via profile, sidewall morphology, and selectivity are discussed.

2.5.1. Various masking materials

The response of positive photoresists investigated for cryogenic etching is shown in Table 1. It appears that 1.3 μm thick PR S1813 is too thin to sustain even a 20 minute etch. To obtain via depths in the range of 100 μm, a requirement for our application, approximately 35 minute etch time is needed. SPR220-3 yields a thickness of 1.9 μm at 3000 rpm, a minimum spin speed to avoid problems with film uniformity. This resist not only exhibits significant cracking, as shown in Figure 2.1, but the film does not sustain a 35 min etch due to poor selectivity. PR S1827, 2.7 μm thick, also exhibits cracking after a 35 min etch. Even though photoresist cracking occurs, tapered via profiles can be obtained with resists as mask materials although reliability would likely be an issue.
Table 2.1. Investigation of various photoresists as masking materials for cryogenic etching.

<table>
<thead>
<tr>
<th>Photoresist</th>
<th>Thickness (µm)</th>
<th>Etch Time (min)</th>
<th>Observation</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR S1813</td>
<td>1.3</td>
<td>35</td>
<td>All resist etched away</td>
</tr>
<tr>
<td>SPR220-3</td>
<td>1.9</td>
<td>35</td>
<td>All resist etched away</td>
</tr>
<tr>
<td>PR S1813</td>
<td>1.3</td>
<td>25</td>
<td>All resist etched away</td>
</tr>
<tr>
<td>SPR220-3</td>
<td>1.9</td>
<td>25</td>
<td>PR Cracked</td>
</tr>
<tr>
<td>PR S1813</td>
<td>1.3</td>
<td>20</td>
<td>All resist etched away</td>
</tr>
<tr>
<td>SPR220-3</td>
<td>1.9</td>
<td>20</td>
<td>PR Cracked</td>
</tr>
<tr>
<td>PR S1827</td>
<td>2.7</td>
<td>35</td>
<td>PR Cracked</td>
</tr>
</tbody>
</table>

Figure 2.1. Top view of a sample etched with a 1.9 µm thick photoresist mask (SPR220-3) showing cracking of PR that results from low temperature exposure.

It is believed cracking occurs due to stresses sustained during thermal cycling [26, 27]. Thinner films have better stress tolerance [24] making thick films more susceptible to cracking. Because of the cracking issues associated with resists, only hard mask materials were considered for further studies. Unfortunately, silicon spikes are generated with Al
masks due to micromasking [25]. For the same etch parameters, SiO2 masks yield a slightly higher etch rate with less undercut and bowing than both Al and Cr masks. For this reason, only SiO2 masks were used in etching vias in this study with a critical 87° sidewall angle, an angle appropriate to ensure conformal deposition of the lining materials before copper filling.

2.5.2. Effect of oxygen flow in the gas mixture

The percentage of oxygen in the SF6/O2 gas mixture plays a crucial role in defining via profile. To investigate this effect, the flow of oxygen was varied while keeping other parameters constant. The process parameters were: substrate temperature of -100 °C; chamber pressure of 12 mTorr; ICP power of 700 W; rf power of 3 W; etch time of 35 min; SF6 flow rate of 36 sccm. Oxygen gas flow was varied (4, 5, and 6 sccm) resulting in three percentages of oxygen in the gas flow mixture of (10, 12, and 14 %, respectively). By increasing the amount of oxygen, passivation of the via sidewall is increased and tapering can be achieved. However, increasing the percentage of oxygen in the gas mixture leads to some reduction in the etch rate. Figure 2.2 shows both variation of via sidewall angle and etch rate as a function of the amount of oxygen in the gas mixture. Changing the percentage of oxygen in the gas mixture from 10 % to 14 % reduces the etch rate from 3.6 to 3.0 μm/min. The reduction in etch rate is believed to result from a growth of the SiOxFx inhibiting film which occurs only when the O2 ratio is high enough to replace fluorine leading to a reduction of reacting species [28, 29]. For low O2 concentrations, sulfur is present on the surface and prevents oxygen atoms from adsorbing.
Variation of via sidewall angle and etch rate as a function of the amount of oxygen in the SF$_6$/O$_2$ gas mixture.

Other studies showed the formation of the SiO$_x$F$_y$ layer leads to a reduction in the etch rate because it prevents the formation of the etch products [30, 31].

When the percentage of oxygen in the gas mixture is less than 10 %, a straight sidewall (90 ° sidewall angle) results. A tapered profile (88° sidewall angle) is obtained by increasing the percentage of O$_2$ to 14 % in the gas flow. The formation of silicon grass was observed although was substantially reduced by increasing the substrate temperature from -100 to -90 °C as the threshold in oxygen content for its formation has been shown to increase with temperature [32, 33].

2.5.3. Effect of substrate temperature

Substrate temperature is another key parameter affecting via profile. Previous studies show the SiO$_x$F$_y$ passivating layer to be extremely sensitive to temperature [11].

The effect of temperature on the via sidewall profile was investigated by using the baseline process parameters given in Table 2.2 and varying the substrate temperature.
Table 2.2. Process parameters used to investigate the effect of substrate temperature on via profile.

<table>
<thead>
<tr>
<th>Process parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chamber pressure (mTorr)</td>
<td>12</td>
</tr>
<tr>
<td>ICP power (W)</td>
<td>700</td>
</tr>
<tr>
<td>rf forward power (W)/dc bias (V)</td>
<td>3/9</td>
</tr>
<tr>
<td>SF$_6$ flow rate (sccm)</td>
<td>36</td>
</tr>
<tr>
<td>O$_2$ flow rate (sccm)</td>
<td>4</td>
</tr>
<tr>
<td>Helium backing pressure (Torr)</td>
<td>10</td>
</tr>
<tr>
<td>Etch time (min)</td>
<td>35</td>
</tr>
<tr>
<td>Temperature range (°C)</td>
<td>-130, -120, -100, -90, -80</td>
</tr>
</tbody>
</table>

The results of this experiment are shown in Figure 2.3.

![Graph showing via sidewall angle versus substrate temperature.](image)

Figure 2.3. Via sidewall angle versus substrate temperature.

When the temperature is increased from -130 to -100 °C, via sidewall angle decreases from 94 ° (negative tapering) to 90 ° (straight sidewall). Negative tapering refers to the via base possessing a larger diameter than the via opening. Positive tapering is achieved
when the substrate temperature is increased to values of -90 and -80 °C. These results are in agreement with the published guidelines from a previous study investigating optimization of profiles [13].

The general trend indicates substrate temperature needs to be increased in order to achieve the desired positive tapering. Cross sectional images are shown in Figure 2.4 for various substrate temperatures. Our goal is to obtain a slightly tapered profile (87° sidewall angle) while maintaining a reasonable etch rate. This profile is suitable in achieving that goal. The small amount of tapering required for conformal via lining leads to a slight increase in via diameter and therefore a reduced pitch. This fact, however, does not eliminate high via density applications.

![Figure 2.4](image)

**Figure 2.4.** SEM cross sectional images of via profiles after cryogenic etching for 35 min using a SiO₂ mask at (a) -130 °C, 81 μm in depth; (b) -100 °C, 116 μm in depth and 45 μm diameter; (c) -90 °C, 108 μm in depth, 30 μm (top), and 24 μm (bottom) diameters; d) -80 °C, 104 μm in depth, 35 μm (top), and 25 μm (bottom) diameters.

Another advantage to using -90° C substrate temperature is the expected reduction in silicon grass formation when the temperature is increased while maintain the same percentage of oxygen as previously reported [25]. Other parameters which have less
impact on the via profile were investigated for their effect on etch rate and mask selectivity.

2.5.4. Effect of chamber pressure

To investigate the effect of chamber pressure on etch rate and selectivity of hard mask materials, pressure values are varied in the baseline recipe. Process parameters include: substrate temperature -100 °C; ICP power 700 W; rf power 3 W; SF$_6$ flow rate 36 sccm, O$_2$ flow rate 4 sccm; and etch time 35 min. Chamber pressure is varied from 8 to 20 mTorr. Etch rates for SiO$_2$, Cr, and Al masking materials are determined using etch depth and etch time. Average etch rate versus chamber pressure, including standard deviation values, is shown in Figure 2.5. Etch rate increases with increasing chamber pressure in the pressure range under study. At low pressures, where ion flux is high, only the availability of F-radicals can limit the etching process as observed in previous studies [18, 19]. In our study, we found a maximum etch rate of 4.03 μm/min, a value that is near the limit of the capability of the equipment. While it would seem advantageous to continue to increase the pressure, the higher the pressure the more difficult it is to control the profile. For this reason, our studies on profile control use a value of 12 mTorr for chamber pressure in the baseline recipe.
From Figure 2.5, a slightly higher etch rate is observed for a SiO$_2$ mask compared to both Al and Cr. Etch rate also increases when via diameter is slightly increased while using a SiO$_2$ mask (3.40 μm/min for 22 μm diameter and 3.60 μm/min for 27 μm diameter). This is due to the fact that the mean free path of reacting species increases with via diameter and collisions with the via sidewall regulate the transport mechanism.

Another parameter investigated is the etch selectivity as a function of chamber pressure. Selectivity versus chamber pressure for a SiO$_2$ mask material is shown in Figure 2.6. Selectivity increases with increasing pressure in the same way that Gomez et al. observed for the same pressure range [20].
Figure 2.6. Selectivity of SiO$_2$ masking material versus chamber pressure.

This trend is due to the fact that at low pressures, both ion flux and oxide sputtering rates are high. Etching of silicon is limited by fluorine radicals, as mentioned previously, at the same time when an increased etching of oxide occurs due to higher sputtering rate at the surface. As the pressure increases, more radicals are available to etch silicon resulting in increased selectivity.

2.5.5. Effect of ICP power

ICP power is a parameter that does not have a large impact on sidewall slope although does have a significant effect on etch rate. This parameter was investigated by varying values from 500 to 1000 W using a SiO$_2$ mask and the baseline recipe parameters: pressure 12 mTorr; temperature -100°C; rf power 3 W; SF$_6$ flow rate 36 sccm, O$_2$ flow rate 4 sccm; and etch time 35 min. Silicon etch rate and mask selectivity as a function of ICP power is shown in Figure 2.7. Etch rate values are 2.71, 3.32, and 3.06
μm/minute for power settings of 500, 700, 1000 W, respectively. Etch rate peaks at 700 W.

Figure 2.7. Silicon etch rate and SiO₂ mask selectivity as a function of ICP power.

Others have observed, at a pressure of 10 mTorr, etch rate to increase with ICP power until saturation occurs at approximately 750 W [13]. Our observation could be a similar phenomenon. In this experiment, a SiO₂ mask was once more found to yield a slightly higher etch rate than metal masks. Measured etch rates were: 2.71 μm/min for SiO₂; 2.54 μm/min for Al; and 2.43 μm/min for Cr at 500 W. This result is consistent with our observations that show a reduction in etch rate when switching from SiO₂ to Al and Cr masks. For an oxide mask, selectivity is found to decrease with increasing ICP power. This is believed to be due to an increased sputtering at the surface as the ICP power is increased.
2.5.6. Process recipe

After exploring the effect of process parameters on both sidewall profile and silicon etch rate, the recipe for etching the desired via profile for TSV applications is shown in Table 2.3. Profiles obtained with this recipe and four different masking materials are shown in Figure 2.8. Al yields a large density of silicon spikes due to micromasking.

Table 2.3. Process parameters used to etch tapered vias (sidewall angle 87°) to be used in TSV applications.

<table>
<thead>
<tr>
<th>Process parameters</th>
<th>values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chamber pressure (mTorr)</td>
<td>12</td>
</tr>
<tr>
<td>ICP power (W)</td>
<td>700</td>
</tr>
<tr>
<td>rf forward power (W)/dc bias (V)</td>
<td>3/9</td>
</tr>
<tr>
<td>SF$_6$ flow rate (sccm)</td>
<td>36</td>
</tr>
<tr>
<td>O$_2$ flow rate (sccm)</td>
<td>6</td>
</tr>
<tr>
<td>Helium backing pressure (Torr)</td>
<td>10</td>
</tr>
<tr>
<td>Etch time (min)</td>
<td>35</td>
</tr>
<tr>
<td>Temperature (°C)</td>
<td>-90</td>
</tr>
</tbody>
</table>
Figure 2.8. SEM cross sectional images of tapered vias (sidewall angle 87 °) for TSV applications obtained with four masking materials: (a) SiO$_2$, (b) Al, (c) Cr (illustrating bowing), and (d) PR S1827 (illustrating the effect of cracks). The vias are 100 μm in depth, 29 μm (top), and 21 μm (bottom) in diameter.

The use of a Cr mask results in bowing at the top of the via and the SiO$_2$ mask yields the best overall profile. These profiles were also inspected for silicon grass formation which appears only on large feature sizes. This aspect is illustrated in Figure 2.9 by SEM images. The larger feature sizes are simply alignment marks used in our process to indicate the wafer thinning process is nearing completion. Because alignment marks are larger than the vias, they are etched deeper and become a useful way to determine a stopping point for the wafer thinning process [34].
Using the cryogenic etch recipe resulting from these studies, vias are etched and the sidewalls are subsequently lined with insulation, barrier, and seed films. Silicon dioxide (2 μm) is deposited by PECVD while a titanium barrier layer (0.25 μm) and copper seed layer (2 μm) are sputter deposited. Electrodeposition is used to fill the vias with copper.

An optical microscope image, Figure 2.10, shows the cross section of a copper filled via. The filling parameters for the electroplating process using reverse periodic pulse plating are shown in Table 2.4.
Table 2.4. Electroplating parameters used to fill vias with copper.

<table>
<thead>
<tr>
<th>Plating steps</th>
<th>Pulse waveform (ms)</th>
<th>Current density (mA/cm²)</th>
<th>Plating time (Min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 1 (DC)</td>
<td>Continuous</td>
<td>4</td>
<td>1.5</td>
</tr>
<tr>
<td>Step 2 (AC)</td>
<td>100 (Fwd), 10 (Rev)</td>
<td>4 (Fwd) &amp; 10 (Rev)</td>
<td>120</td>
</tr>
<tr>
<td>Step 3 (AC)</td>
<td>100 (Off)</td>
<td>8 (Fwd) &amp; 10 (Rev)</td>
<td>120</td>
</tr>
</tbody>
</table>

2.6. Conclusions

Substrate temperature and percentage of oxygen in the gas mixture are found to be key parameters affecting the via sidewall angle. A tapered via profile with 87° angle is obtained using a substrate temperature of -90 °C and 14 % oxygen in the SF₆/O₂ mixture. With the resulting process recipe, silicon grass is found to be substantially reduced for feature sizes used in our application. Etch rates as high as 4 μm/min, for a 35 minute etch, are reached through careful selection of process parameters. Positive photoresist, thicker than 1.3 μm, is found to be more prone to cracking at cryogenic temperatures necessitating a hard mask for deep etching. From the three hard mask materials used in
In this study, Al yields a large density of silicon spikes due to micromasking, a Cr mask generates bowing at the top of the via, with a SiO₂ mask yielding the best overall profile. This mask material is used in our study to produce tapered via sidewalls. The silicon etch rate increases with pressure in a chemical-limited reaction regime up to chamber pressures of 20 mTorr where the highest etch rate is observed before decreasing in a physical-limited reaction regime beyond this pressure value. As chamber pressure is increased beyond these values, it becomes more and more difficult to control the via profile. Finally, mask selectivity decreases with an increase in ICP power and increases with chamber pressure up to a value of 20 mTorr.

Acknowledgements

This work is supported by the College of Engineering and the Central Analytical Facility at the University of Alabama. Use of the Center for Nanoscale Materials at Argonne National Laboratory is supported by US DOE contract No. DE-AC02-06CH11357.

2.7. Chapter 2 References


CHAPTER 3

RELIABILITY STUDY OF THROUGH-SILICON VIA (TSV)

COPPER FILLED INTERCONNECTS**

Abstract

Through-silicon vias (TSVs) have been extensively studied because of their ability to achieve chip stacking for enhanced system performance. The fabrication process is becoming somewhat mature. However, reliability issues need to be addressed in order for an eventual transition from laboratory to production. In our laboratory, vias with tapered sidewalls are formed through a modified Bosch process using deep reactive ion etching (DRIE). Vias are lined with silicon dioxide using plasma enhanced chemical vapor deposition (PECVD) followed by sputter deposited titanium barrier and copper seed layers before filling with a reverse pulse copper electroplating process. Following attachment of the process wafer to a carrier wafer, the process wafer is thinned from the backside by a combination of mechanical methods and reactive ion etching (RIE). Fabricated vias are subjected to thermal cycling with temperatures ranging from -25 °C to 125 °C. For via chains, erratic changes in resistance upon temperature cycling indicated a problem with the wire bonds used to connect the sample to the test fixture. Test methods were modified to avoid wire bonding and form the basis of reliability studies presented in this paper. TSVs are shown to be stable with small increases in measured resistance for 200 cycles. In addition, small changes in resistance are observed when vias are held at elevated temperatures for extended periods of time.

3.1. Introduction

Metal filled through-silicon vias (TSVs) allow devices to be connected using a three dimensional (3-D) approach. Optimizing and refining this technology has been a focus for the semiconductor industry the past few years because of the need for novel integrated circuit (IC) packages that can address the issues associated with increased functionality and performance while reducing size and costs for a growing number of defense and consumer electronics applications [1-3]. This technology will be adopted for many applications in the future because of the capability in solving problems related to electrical performance, memory latency, power and noise on-and off-chip. An application of TSVs in production today involves CMOS image sensors where the active silicon area is bonded onto glass and contacted from the backside [4-8]. TSVs for stacked chip applications are under development with the goal of enabling integration of complex systems [9-13]. Different packaging approaches are used to perform 3-D system integration that include: system in package (SiP); system on chip (SoC); and system on package (SoP) [14]. TSV is a very promising technology that may replace wire bonding in SiP, SoP, as well as chip stacking technologies [15-19]. Different materials and methods have been proposed and tested for TSV applications, but feature dimensions, final material deposit characteristics and process reliability are the main limiting factors to the application of these materials and methods, along with typical cost considerations [1, 20]. Copper is the most common material used to fill vias because of its low electrical resistance and compatibility to conventional multilayer interconnects. Even though it is difficult to fill high aspect ratio vias without voids through conventional damascene electroplating, several approaches have been developed. They typically involve
optimization of the electroplating bath, the reverse pulse waveform, and the current
density [21-22]. This paper focuses on thermal cycle testing of TSVs that previous DC
tests show to be high in yield and electrically reliable [23].

3.2. Temperature Cycling

Temperature cycling determines the ability of devices to maintain operation at
extremely low and high temperatures, as well as their ability to withstand exposure to
these temperatures in a cyclic manner. Both temperature cycling and thermal shock
accelerate fatigue failures depending on the temperature ranges, the transfer time between
the two temperatures, and the dwell times at the extreme temperatures. For reliability
testing when qualifying new devices, up to 1000 temperature cycles are usually
performed with interim visual inspection and electrical tests at 200 and 500 cycles [24-
26]. Several different ranges of temperatures are used in temperature cycle testing
depending on the application. Some researchers consider only positive temperature
ranges while others consider wider ranges more consistent with operation in a cold
environment. Reliability tests have been conducted on solder joints [27], copper wires
[28], and lead-free flip chip assemblies using direct under-filling by transfer molding
[29]. From these studies, the appearance of cracks may be detected in some materials or
structures after less than 100 cycles (e.g., the case of transfer molding used in lead-free
flip chip assemblies) even though other materials are able to withstand 12,000 cycles
without failure. Fortunately, copper filled microstructures appear to be more robust with
no major changes observed in electrical resistance values below 200 cycles [26].
3.3. **Experimental Procedures**

This section is organized by discussion of the fabrication of TSVs (sections 3.3.1-3.3.5) and testing of the vias (section 3.3.6). Completed TSV dimensions are diameters of approximately 45 μm and depths of 95 μm. Three test configurations are formed when fabricating TSVs to measure: single via resistance; via chain resistance (chains of 48 and 72 vias); and insulation between vias.

3.3.1. **Formation of blind vias**

The process of forming vias is conducted using an STS deep reactive ion etch (DRIE) tool and 8 μm thick photoresist layer as the mask material. A modified Bosch process is used that allows blind vias to be formed with a slight sidewall taper (sidewall angle = 83°). The taper is necessary to create a wider opening at the top of the via for ease in depositing materials that line the via. A typical Bosch process produces vias with straight sidewalls. The modification in our Bosch recipe comes from adjusting passivation cycle times in order to change the amount of passivation material that is available to protect the sidewalls throughout the etch [30]. Recipe power settings are 12 W platen power in the etch cycle, 0 W in the passivation cycle and 200 W coil power for both etch and passivation cycles. Other process parameters are provided in Table 3.1. A cross section of the via after etching is shown in Figure 3.1. At the end of the etch process, a piranha solution consisting of a 3:1 mixture of concentrated sulfuric acid (H₂SO₄) with hydrogen peroxide (H₂O₂) removes the remaining photoresist.
Table 3.1. Processing parameters used for DRIE to form blind vias with tapered sidewall.

<table>
<thead>
<tr>
<th>Recipe for 83° sidewall via profile</th>
<th>Etching/Passivation cycles (sec)</th>
<th>Number of cycles for each module = 37</th>
<th>APC angle (degree)</th>
<th>Gas flow (SCCM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mod 1</td>
<td>18/6</td>
<td>50</td>
<td>112</td>
<td>130</td>
</tr>
<tr>
<td>Mod 2</td>
<td>18/7</td>
<td>60</td>
<td>112</td>
<td>85</td>
</tr>
<tr>
<td>Mod 3</td>
<td>18/9</td>
<td>60</td>
<td>112</td>
<td>85</td>
</tr>
<tr>
<td>Mod 4</td>
<td>18/11</td>
<td>60</td>
<td>112</td>
<td>85</td>
</tr>
<tr>
<td>Mod 5</td>
<td>18/13</td>
<td>60</td>
<td>112</td>
<td>85</td>
</tr>
<tr>
<td>Mod 6</td>
<td>18/15</td>
<td>60</td>
<td>112</td>
<td>85</td>
</tr>
<tr>
<td>Mod 7</td>
<td>18/17</td>
<td>60</td>
<td>112</td>
<td>85</td>
</tr>
<tr>
<td>Vias depth (µm)</td>
<td></td>
<td>95</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.1. Cross sectional image showing a blind via profile obtained after DRIE etching.

3.3.2. Deposition of insulation, barrier, and seed layers

A silicon dioxide (SiO$_2$) layer, 2 µm in thickness, is deposited at 250 °C using a plasma enhanced chemical vapor deposition (PECVD) system. This provides the via insulation layer. Sputtering titanium (0.5 µm) to serve as a barrier layer is performed at a
pressure of 0.6664 Pa and 2500 W. This is followed by sputtering a copper seed layer (2 μm) at the same pressure and a power setting of 3000 W. The sputtering process begins with a 60 sec RF etch to clean the wafer surface. Insulation, barrier, and seed layers that are lining the via need to be as conformal as possible for appropriate coverage.

Parameters for via filling by periodic reverse pulse electroplating and formation of the test pads by DC electroplating are shown in Table 3.2.

Table 3.2. Electroplating parameters used to fill vias (front side) and to fabricate testing pads (back side).

<table>
<thead>
<tr>
<th>Metals plated</th>
<th>Front side</th>
<th>Back side (Testing Pad)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cu Filling</td>
<td>Cu</td>
</tr>
<tr>
<td>Pulse Waveform (ms)</td>
<td>Fwd</td>
<td>100</td>
</tr>
<tr>
<td>Rev</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Off</td>
<td>100</td>
<td>1.5</td>
</tr>
<tr>
<td>Current density (mA/cm²)</td>
<td>5 (DC)</td>
<td>10</td>
</tr>
<tr>
<td>5 (Fwd) &amp; 10 (Rev)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>10 (Fwd) &amp; 10 (Rev)</td>
<td>11</td>
<td>3</td>
</tr>
<tr>
<td>Plating Time (Min)</td>
<td>120</td>
<td>60</td>
</tr>
</tbody>
</table>

3.3.3. Via filling

Electroplating is used to fill the vias starting with a short 90 sec DC plating step at a current density of 5 mA/cm². This short plating step has been shown to reinforce the seed layer [31] before switching to periodic reverse pulse plating. Optimizing the plating process helps to achieve void-free filling. Our approach to this optimization includes: use of a fountain plating system that provides agitation and allows the plating solution to reach the base of the vias; control of organic additives; and use of appropriate current density levels [32, 33]. The settings for pulse plating begin with a forward current density of 5 mA/cm² for 100 ms, a reverse current density of 10 mA/cm² for 10 ms and 100 ms.
with no applied current (off time) to allow solution stabilization. When the vias are approximately half filled, the forward current density is increased to 10 mA/cm$^2$ for the remainder of the via filling process. The change in forward current density levels is done to address the fact that the aspect ratio is changing as the via fills with metal in a bottom-up manner.

3.3.4. **Wafer attachment and thinning**

Following the electroplating step, the filled blind vias will become through-silicon vias by mechanically thinning the wafer from the backside. Because the process wafer will be thinned, a carrier wafer is used for handling purposes. A liquid crystal polymer (LCP) film serves as the laminating material for the two wafers using a PHI compression system with a 12.5 ton force applied at 300 °C. The resulting stacked wafers have a planarity of ± 2 μm and exhibit strong bonding that will hold up to the backside thinning process.

A Logitech PM5 lapping system is used to remove the bulk of the silicon from the process wafer with a 15 μm aluminum oxide abrasive grit. The material removal rate is nearly uniform over time at 3.2 μm/min for a lapping plate rotation of 70 rpm as shown in Figure 3.2. During the lapping process, good planarity is achieved by controlling the lapping plate flatness through periodic conditioning. Alignment marks on the process wafer are used to terminate the grinding process as they are larger than via feature dimensions and are therefore etched deeper [34]. At this point a finer abrasive grit (0.3 μm) is used for mechanical polishing with a removal rate of 0.1 μm/min for a sample jig rotating at 45 rpm.
Figure 3.2. Silicon bulk material removal as a function of lapping time.

3.3.5. Wafer backside processing

A reactive ion etch (RIE) system is used to etch the remaining silicon which will expose the base of the via. Contact pads can be formed by removing the insulation layer at the via base and electroplating metal. Pads are fabricated by electroplating 2 μm of copper using a current density of 10 mA/cm$^2$ followed by electroplating 2 μm of nickel using a current density of 40 mA/cm$^2$. Electroplating nickel-strike (0.5 μm) promotes Ni-Au adhesion and is done at a current density of 10 mA/cm$^2$ before completing the pad with 2 μm of gold at a current density of 1.5 mA/cm$^2$.

3.3.6. Thermal cycling for reliability studies

Thermal cycling tests are conducted using a model 6000 Physical Property Measurement System (PPMS) designed to perform a variety of automated measurements.
The PPMS sample mounting system is an interesting feature of this instrument having a 12-pin connector pre-wired to the system electronics at the bottom of the sample chamber. This connector allows one to plug in a removable sample insert offering convenient access to electrical leads. To control the temperature, a vacuum pump draws helium into an annular region where heaters can also warm the gas to the correct temperature. One of our test configurations has many vias connected in a daisy chain and resistance was measured in this experimental setup using the Van der Pauw principle. Initially, sample preparation included wire bonding and for this purpose, a West Bond Inc. model 7400 C wire bond system was used. For cycling experiments, a maximum temperature ramp rate of 20 °K/min was used with temperatures in the range of -25 °C to +125 °C and measurements were taken every 5 °C while ramping in both temperature directions. Upon reaching both maximum and minimum temperatures, a 5 minute dwell time was observed before starting the next cycle.

3.4. Results and Discussion

Figure 3.3 shows an image of the contact pads for different test structures used to investigate reliability of the vias. Single via resistance, daisy chain via resistance, and insulation between vias was determined. From insulation tests over the entire wafer, the measured resistance was greater than 80 MΩ. Single via tests measured an average resistance value of 8 mΩ uniformly over the wafer. These results are in good agreement with previously tested single vias of the same diameter where an average value of 13 mΩ was measured. Using some assumptions regarding via profile, a theoretical value of 5 mΩ
is obtained [32]. For different via daisy chain lengths, the test results are shown in Table 3.3.

![Image](image.png)

**Figure 3.3.** Cross section of fabricated TSVs showing vias connection on both front and back sides.

**Table 3.3.** Daisy chain resistance measurements for fabricated TSVs

<table>
<thead>
<tr>
<th>Measured via chain resistance (Ω)</th>
<th>72 Vias</th>
<th>0.6</th>
<th>0.5</th>
<th>0.6</th>
<th>0.5</th>
<th>0.5</th>
<th>0.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>48 Vias</td>
<td>0.2</td>
<td>∞</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>72 Vias</td>
<td>0.3</td>
<td>0.4</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>48 Vias</td>
<td>0.3</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>72 Vias</td>
<td>0.6</td>
<td>0.4</td>
<td>0.6</td>
<td>0.4</td>
<td>0.2</td>
<td>∞</td>
<td></td>
</tr>
<tr>
<td>48 Vias</td>
<td>0.4</td>
<td>0.3</td>
<td>0.4</td>
<td>0.2</td>
<td>0.2</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>72 Vias</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>48 Vias</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.4</td>
<td>0.2</td>
<td>0.2</td>
<td></td>
</tr>
</tbody>
</table>

**Theoretical via chain resistance (Ω)**

| 72 vias                          | 0.33    |
| 48 vias                          | 0.24    |

We observed a discontinuity for two chains that were further probed to identify vias with open circuits. For each of these chains, only one via was observed to be faulty out of a total of 2880 vias, resulting in a 99.93% yield for the tested vias. Figure 3.4
shows a cross section of daisy chained vias connected on both front and back sides. Overall, electrical testing shows that vias fabricated by our process flow exhibit high yield and low resistance values.

Figure 3.4. Cross section of fabricated TSVs showing vias connection on both front and back sides.

Another reliability issue investigated in this paper was the response of vias to thermal cycling. In this approach, it is of interest to observe how sensitive via resistance is to successive temperature cycling. For via chains, 240 in length, resistance as a function of temperature when ramping up the temperature for seven cycles is shown in Figure 3.5. Resistance when ramping down the temperature is shown in Figure 3.6.

Figure 3.5. Chain resistance of 240 vias as a function of temperature (ramping up).
Figure 3.6. Chain resistance of 240 vias as a function of temperature (ramping down).

The plot labeled “R1 up” in the open circle symbol depicts increasing resistance measured during the first cycle as the temperature is increased from 248 to 398 °K (Figure 3.5). Once that temperature is reached and stable, resistance is measured while temperature is decreased and that plot is labeled “R1 down” in the open circle symbol (Figure 3.6). The second cycle is shown in Figure 3.5 on the plot labeled “R2 up” in the open square symbol and depicts increasing resistance as the temperature is increased followed by the plot labeled “R2 down” in the open square symbol and so on. For simplicity, Figure 3.7 shows the resistance as a function of temperature for the first and seventh cycles only for both increasing and decreasing temperatures.
Figure 3.7. Chain resistance of 240 vias as a function of temperature for the first and seventh cycles.

The data shown in Figures 3.5-3.7 indicate that via resistance increased significantly even in the first cycle, an unexpected result. The wire bonds were investigated as a source of the increasing resistance by removing the wires and re-bonding before testing resistance again. Following this procedure, measured via chain resistance had decreased to the original value. We concluded that faulty wire bonds were the major contribution to the increasing resistance as the temperature was cycled back and forth. For this reason, longer cycling runs (200 cycles) were conducted without attaching wire bonds until after the temperature cycling was complete, immediately before measuring the resistance. Thermal cycling test results are shown in Table 3.4 for via chains with no wire bonds present during temperature cycling (200 cycles).
Table 3.4. Resistance measurements for thermal cycling (200 cycles).

<table>
<thead>
<tr>
<th>Via Chain Resistance (Ω)</th>
<th>Initial (N =0)</th>
<th>Final (N =200)</th>
<th>% Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>2.36</td>
<td>2.41</td>
<td>2.12</td>
</tr>
<tr>
<td>Sample 2</td>
<td>2.71</td>
<td>2.79</td>
<td>2.95</td>
</tr>
<tr>
<td>Sample 3</td>
<td>2.57</td>
<td>2.64</td>
<td>2.72</td>
</tr>
</tbody>
</table>

Resistance values change in the range of 2-3 % and no discontinuity in via chains was observed. Cycling was not increased to over 200 runs due to the large amount of helium required for this test procedure.

High temperature storage tests were carried out on TSVs to investigate the effect of an increased temperature on via electrical resistance over time. Samples (240 daisy chained vias) were simply stored at elevated temperatures and resistance was measured before and after storage. Via chain resistance is shown in Table 3.5. From this type of test it appears that vias can sustain up to 250 °C for 200 hrs with less than a 10 % increase in resistance.

Table 3.5. Resistance measurements from high temperature storage tests.

<table>
<thead>
<tr>
<th>Via Chain Resistance (Ω)</th>
<th>Initial Value</th>
<th>At T=150°C for 48 hrs</th>
<th>At T=150°C for 120 hrs</th>
<th>At T=250°C for 48 hrs</th>
<th>At T=250°C for 120 hrs</th>
<th>At T=250°C for 200 hrs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>2.42</td>
<td>2.50</td>
<td>2.52</td>
<td>2.57</td>
<td>2.59</td>
<td>2.63</td>
</tr>
<tr>
<td>Sample 2</td>
<td>2.28</td>
<td>2.36</td>
<td>2.37</td>
<td>2.42</td>
<td>2.44</td>
<td>2.47</td>
</tr>
</tbody>
</table>

3.5. Conclusions

Through-silicon vias (TSVs) were fabricated and resistance was measured for both single vias and long via chains. Insulation tests were also conducted. The vias were found to be well insulated with measured yields on the order of 99.93 %. These vias were
further investigated for reliability through temperature cycling with temperatures ranging from -25 °C to 125 °C. Wire bonds were found to be the source of increasing resistance during thermal cycling so cycling runs were performed with bonding performed only immediately before and immediately after the temperature cycles. When temperature cycling (200 cycles) was conducted, small changes in via chain resistance were observed with preservation of via chain continuity. Investigation of the discontinuity observed between two vias revealed through sample polishing and imaging that this problem was surface-related. The vias appear to be stable to temperature cycling. Similar results were obtained following storage of vias at temperatures as high as 250 °C for 200 hrs with no large increase in resistance measured.

Acknowledgements

The authors would like to acknowledge the support of the United States Air Force Research Laboratories under grant FA8650-04-2-1619. The assistance of Madhav Rao, Dr. Patrick Leclair, and Dr. Sushma Kotru from the Materials for Information Technology (MINT) Center at the University of Alabama for wire bonding, cycling and thermal shock measurements is greatly appreciated. The assistance of the technical staff at the High Density Electronics Center at the University of Arkansas is also acknowledged.

3.6. Chapter 3 References


ADDENDUM TO CHAPTER 3
INVESTIGATING DEFECTS IN THROUGH-SILICON VIA CHAINS BY
THREE-DIMENSIONAL IMAGING RECONSTRUCTION***

Discontinuities in two via chains were further investigated by first probing the vias and alternating a series of polishing and imaging steps to determine the location and nature of the failures. The polishing was performed along both the diameter and depth of the vias. Three dimensional imaging reconstruction allowed investigation of the defects. Samples were diced and mounted using a Simplimet 1000 automatic mounting press operated at 4200 psi. A Roto Pol-22 was used for polishing using a lubricant and suspension supplied automatically by a multidoser. A two-step polishing process using both a MD-largo pad and a MD-Dac fine grit pad for one minute each was used repeatedly. The two plates were set to rotate at 300 and 150 rpm respectively, while a 20 N force was applied. Each step was followed by sample cleaning and imaging of the same area using an optical microscope.

Approximately 40 images were collected from the backside pad through the via depth and the front-side pad for one sample. A set of images collected during the process is shown in Figure 3.8.

*** This work was presented at the TMS conference in Seattle WA, February 10-14, 2010 as: A. Kamto, R. Morris, G. B. Thompson, and S. L. Burkett, “Investigating defects in through silicon via chains by three dimensional imaging reconstruction.”
Figure 3.8. Optical images collected from the polishing process showing: backside pad (a-c), vias in the silicon substrate (d-e), front-side pad (f-h). The arrows refer to the discontinuity between two vias on the pad.

The same process was carried out with a via cross-section polishing for the second sample as shown in Figure 3.9. The polishing process revealed that the discontinuity between two vias was a surface defect (pad level) confirming the robust nature of these vias as described in the previous sections. Each of the images represents a layer in the 3D imaging reconstruction process using Amira software. Amira is a 3D visualization and modeling system that allows visualization of scientific data sets from various applications, e.g. medicine, biology, chemistry, physics, or engineering. It allows representation of 3D objects as grids suitable for numerical simulations and includes a general purpose interactive 3D viewer.
Figure 3.9. Optical images collected from the polishing of via cross-section showing two adjacent pads with: a) no via exposed, b) one via exposed on the first pad, c) both vias exposed on the first pad, both vias exposed on the two pads.

The system obtained following 3D imaging reconstruction is shown in Figure 3.10. The defect would have been clearly observed if it had been located inside the via. For example, a void in the filling process would have been inside in the cross section revealed by this sequence of polishing and imaging steps.
Figure 3.10. Three-dimensional imaging reconstruction using Amira software.
CHAPTER 4
INTEGRATION OF TANTALUM PENTOXIDE CAPACITORS WITH THROUGH-SILICON VIAS (TSVs)

Abstract

Metal filled through-silicon vias (TSVs) allow devices to be connected using a three dimensional (3-D) approach. Optimizing and refining this technology has been a focus for the semiconductor industry the past few years because of the need for novel integrated circuit (IC) packages that address the issues associated with increased functionality and performance while reducing size and costs for a growing number of defense and consumer electronic applications. Vertical interconnection using through-silicon via (TSV) technology has emerged as a convenient way to improve system performance. Integration of decoupling capacitors with TSVs represents an attractive alternative to conventional 2-D layouts to achieve miniaturization and increased density. Decoupling capacitors can be brought in close proximity to the active elements, thereby reducing their parasitic inductance and allowing higher clock rates. In this study, capacitors with anodized tantalum oxide dielectric were integrated with TSVs and their performance was evaluated. Fabricated capacitors were found to exhibit satisfactory electrical properties before and after TSV processing although some changes in their properties were observed. The performance of these capacitors for applications such as high speed decoupling capacitors was evaluated by measuring resonant frequency, parasitic inductance, and parasitic resistance.

**** A manuscript has been submitted for the work in this chapter for publication in IEEE Transactions on Advanced Packaging as: A. Kamto, Y. Liu, S. Jacob, M. Glover, L. Schaper, and S. L. Burkett, “Integration of Tantalum Pentoxide Capacitors with Through-Silicon Vias (TSVs).”
4.1. Introduction

High performance integrated circuits (ICs) demand noise-free power at very short rise times. In advanced packaging applications, the decoupling capacitor is used to supply the instantaneous current required for switching while minimizing the effect of switching noise [1]-[2]. With clock rates continuing to increase, discrete chip capacitors cannot meet the performance requirements because of the large parasitic inductance they generate when operating at high frequencies [3]. Therefore, decoupling capacitors need to be in close proximity to the active elements in order to reduce their parasitic inductance.

Two-dimensional placement of ICs may contain long interconnects, leading to a large signal delay. Vertical interconnection using through-silicon via (TSV) technology has emerged as a convenient way to improve system performance. TSVs, a component of stacked chip systems, have been under development for some time and enable integration of complex electronic systems [4]-[8]. Recent work by our group has shown that TSVs possess good reliability in normal operating conditions [8]-[9].

Several high dielectric constant thin film materials have been studied for use in decoupling capacitors. These materials include barium titanate, perovskite lead lanthanum titanate (PLT), lead lanthanum zirconate titanate (PLZT), lead zirconate, and tantalum oxide. Polycrystalline barium titanate, with a very high dielectric constant (close to 300 at low frequencies), shows dispersion in the GHz frequency range associated with a reduced dielectric constant [10]. Furthermore, it is difficult to deposit ferroelectric films with good electrical properties at temperatures compatible with complementary metal-oxide-semiconductor (CMOS) processing [11]. Amorphous barium titanate does not
show any form of dispersion up to 40 GHz, but has a dielectric constant close to 18 [10].
Tantalum pentoxide (Ta$_2$O$_5$) dielectric films have a dielectric constant close to 25 and can
be deposited by processes that are CMOS compatible (e.g., reactive sputtering or
anodization). Anodization has been shown to form a dense oxide on metallic surfaces,
thereby reducing leakage current values. Potentially integrable decoupling capacitors
based on a planar Ta$_2$O$_5$ dielectric have been studied at the University of Arkansas for
several years [12]-[17].
In this study, TSVs were integrated with capacitors using Ta$_2$O$_5$ as the dielectric in order
to observe the effects of TSV processing on the performance of the capacitors. Ta$_2$O$_5$
dielectric films prepared by anodization of sputtered tantalum (Ta) were found to exhibit
satisfactory electrical properties. TSV processing was found to have minor effects on the
performance of the capacitors fabricated in our laboratory as part of this integration
experiment.

4.2. Background

4.2.1. Tantalum pentoxide capacitors

Ta$_2$O$_5$ dielectric films have received much attention for use in decoupling and
high density memory storage capacitors because of their high dielectric constant ($\varepsilon_r$=25)
[18]. However, Ta$_2$O$_5$ films deposited by conventional methods, such as sputtering and
thermal oxidation, result in low yields and exhibit large leakage currents due to high
defect densities in the films [19]. Oxygen vacancies in the dielectric are believed to
generate capacitor failures thereby impacting initial yield and reliability. A combination
of sputtering and anodization has been found to yield dielectric films exhibiting low
leakage currents, high breakdown fields, and high yields on both silicon and polymeric substrates [12]-[13].

Anodization is the electrochemical oxidation of metals and forms a dense oxide on metallic surfaces. In the anodization process, a metal is placed in a suitable electrolyte and acts as the anode. An oxide layer is formed with the passage of current. The thickness of the oxide layer is controlled by the applied voltage. Anodic films grown on tantalum have been a subject of study for many years because of their practical use as dielectrics. Stable films can be formed on sputter deposited tantalum by anodizing in a suitable electrolyte and this process has commonly been used in the production of capacitors [20].

Capacitors fabricated with dielectrics formed by anodizing metals may exhibit an increase in capacitance upon heating. Smyth et al. presented a theoretical explanation of the oxygen depletion layer to explain why anodized Ta that is heated above 200 °C exhibits increased capacitance and the capacitance has a strong bias, frequency and temperature dependence [21]. Likewise, studies have shown Ta$_2$O$_5$ dissolving into the Ta substrate when annealed under vacuum conditions [21]-[23]. The oxide thickness was found to decrease with the anneal time and the Ta$_2$O$_5$ stoichiometry was essentially unchanged in the remaining layer. This result was obtained following a study of the dissolution process by means of Auger electron spectroscopy (AES) sputter depth profiling for temperatures up to 753 °K [24]. The dissolution process was found to start with the dissociation of Ta$_2$O$_5$ yielding mobile neutral oxygen atoms that are transported according to the magnitude of the diffusion coefficients of oxygen in Ta$_2$O$_5$ and Ta [25]. The oxygen diffusion coefficient has been determined experimentally in both Ta$_2$O$_5$[26]
and polycrystalline Ta [27]. Expressions for these diffusion coefficients, $D_o$, were found to be:

$$D_o(Ta_2O_5) = 4.26 \times 10^{-2} \exp\left(-\frac{42968}{RT}\right) \text{cm}^2 \text{s}^{-1} \tag{1}$$

$$D_o(Ta) = 7 \times 10^{-2} \exp\left(-\frac{25800}{RT}\right) \text{cm}^2 \text{s}^{-1} \tag{2}$$

In these equations, the universal gas constant, $R$, is given in calories per mole per degree Kelvin and the activation energy is given in calories per mole.

From these equations, the diffusion coefficient of oxygen in Ta ($2.25 \times 10^{-9}$ cm$^2$ s$^{-1}$) is about five orders of magnitude larger than the diffusion coefficient of oxygen in Ta$_2$O$_5$ ($1.54 \times 10^{-14}$ cm$^2$ s$^{-1}$) at a temperature of 753 °K. Oxygen diffuses from near the interface towards the Ta substrate following dissociation. As a result, another layer consisting of Ta atoms from the dissolved Ta$_2$O$_5$ exists that essentially moves the interface by the amount of that layer thickness [24]. Another finding was that oxygen deficiency in Ta$_2$O$_5$ could be completely removed by re-anodization through a slow process requiring approximately 5 hours for samples previously heated for 30 min at 450 °C [28].

Chang et al. found that the thermal behavior of Ta$_2$O$_5$ was affected by the presence of surrounding titanium (Ti) having the ability to reduce Ta$_2$O$_5$ at temperatures as low as 400 °C [29]. For this reason, they suggested the use of an oxygen barrier layer in the case where Ti was used in fabricating metal-oxide-metal (MOM) capacitor structures. Two orders of magnitude reduction in leakage current was also observed by substituting TaN/Ta for TiN/Ti in Al/Ta$_2$O$_5$/barrier layer/metal capacitors [29]. Peters et al. used TaN as a diffusion barrier between the Ta$_2$O$_5$ and the aluminum electrode and obtained low leakage currents and low defect densities after exposure to temperatures in the range of 350 °C - 400 °C [30]. Other studies found that both TaN and WN limit oxygen diffusion.
upon exposure of TiO$_2$ to elevated temperatures more effectively than TiN [31]. For these reasons, barrier layers are commonly used in capacitor structures with anodized metals to avoid oxygen diffusion at elevated temperatures. Barrier layers are also commonly used in fabricating through silicon vias to avoid copper migrating through the metal filled via.

4.2.2. Integration of electronic devices with TSVs

TSV processing has become a rather mature technology and is receiving a lot of interest for 3D stacking of devices and systems. This technology is an essential component when integrating devices using a 3D approach. Jozwiak et al. investigated three different process sequences for the integration of pMOSFET devices using through wafer interconnects (TWIs) [32]. Their “bridge process” involved the fabrication of TWIs from the wafer front side following the deposition and patterning of the bond pad metal layer giving the fewest concerns with regard to the integrity of the pre-existing circuitry. Following processing of the TWIs, these devices were tested from the back side of the wafer and the performance was similar to the performance before processing of TWIs. Change in performance was an issue when the TWIs were fabricated from the wafer front side before insertion of the bond pad and when TWIs were processed from the wafer back side [32].

Using TSVs, Taklo et al. combined a fast detector sensor in a 3D package with low parasitic capacitance to generate a radiation detection system with very fast response time [33]. Other studies involved the integration of a 3D microelectromechanical systems (MEMS) sensor and a MEMS bulk acoustic resonator stacked on top of a transceiver for automotive applications. This combination was further stacked on top of a
microcontroller. TSVs in the transceiver were processed using a post back-end-of-line (BEOL) via-first approach and metalized by chemical vapor deposition of tungsten [34]. For the integration of MEMS devices, TSVs were included as either cap wafer TSVs or directly integrated with the MEMS devices depending on the design [33], [35]. A cap wafer represents a protective cover on a semiconductor substrate where one or more devices have been fabricated.

While various planar silicon sensors have been transferred into production lines, research involving 3D integration of silicon devices that may include fragile mechanical parts is still underway. Mori et al. developed an interposer with TSVs used for the integration of an IC chip with embedded thin film resistors, spiral coil inductors, and thin film metal-insulator-metal capacitors. These capacitors had Ta electrodes and Ta$_2$O$_5$ dielectric formed by anodization of Ta. Thin film elements were chosen for high frequency applications where a combination of passive elements was used. Devices were fabricated showing good high-frequency filter properties. Low-pass filters showed signal attenuation at frequencies over 3 GHz and band-pass filters allowed a pass band between 13 and 17.5 GHz [36].

4.3. Experimental Design and Procedures

4.3.1. Mask design

Due to the relatively simple nature of the structures involved, layout for the mask set was accomplished using AutoCAD™. The design consisted of 13 layers, each representing a process mask. Conversion from DXF format into GDSII format was performed using a separate, stand-alone tool (ASM3500 DXF to GDSII bi-directional
Each capacitor cell measures 3 mm × 1.25 mm in size. The cells were arranged on a 125 mm-diameter wafer; allowing for dicing streets, alignment marks, and process monitoring structures. There were a total of 1818 capacitors per wafer. A view of the designed cell for one capacitor is shown in Figure 4.1.

In order to reduce fabrication costs, only three of the photomasks were fabricated on glass substrates. The remaining mask layers were fabricated on photoplot films, which were later attached to glass carriers to allow for proper alignment and exposure. Given the inherent misalignment issues that occur when mixing these two mask types, care was taken to assure that certain feature sizes were oversized to accommodate misalignment. The three masks fabricated on glass were those used to define, expose, and connect to the through-silicon vias from the backside. Precision alignment was critical for these patterning steps to produce viable interconnects.
4.3.2. **Process integration**

In this study, silicon wafers with the following properties were used: n-type phosphorous-doped; resistivity of 4-7 Ω cm; 125 mm diameter; and a thickness of 375 ± 20 µm. The following sections describe the various processing steps used in the integration of capacitors and through-silicon vias.

### 4.3.2.1. Fabrication of tantalum pentoxide capacitors

An oxide (0.5 µm) was deposited by plasma enhanced chemical vapor deposition (PECVD) to insulate capacitors from the bulk silicon. Sputtering of the bottom metal electrode (M$_1$) followed the oxide deposition. This electrode consisted of 500 Å titanium (Ti) and 3 µm thick copper (Cu). Sacrificial layers of both Ti (500 Å) and Cu (1 µm) were added to the Ti/Cu stack to protect the bottom Cu plate from oxidation following the tantalum pentoxide (Ta$_2$O$_5$) dielectric etch in subsequent steps. Tantalum (Ta) sputter deposition (2400 Å) followed the metal electrode sputtering step. All previously mentioned sputtering steps were carried out at a chamber pressure of 5 mTorr and were initiated with a 90 sec RF etch. The power supply settings were 2500 W (Ti), 3000 W (Cu), and 1000 W (Ta). Approximately 2000 Å of the Ta was anodized to yield the Ta$_2$O$_5$ capacitor dielectric. The anodization solution consisted of deionized (DI) water (1500 mL), 99 % ethylene glycol (4000 mL), and 80 g tartaric acid. The process was conducted at a voltage of 125 V and a current of 60 mA. These parameters result in a current density of 0.5 mA/cm$^2$ and growth rate of 16 Å/V. Variation of both current and voltage with time is shown in Figure 4.2. The process starts with the current set at a constant value while voltage increases with time for approximately 15 min when the set value of voltage
is reached. Anodizing current then decreases exponentially for the remaining processing time while the voltage is maintained.

Figure 4.2. Anodization current and voltage as a function of time.

After forming the dielectric, the top metal electrode (M₂) was sputter deposited. This top electrode consisted of a Ti/Cu/Ti stack where each Ti layer was 500 Å thick and the Cu was 3 µm in thickness. The top layer of Ti protects the underlying Cu from oxidation. After sputtering Ti/Cu/Ti, the first three photomasks were used to successively pattern and etch the top electrode, the Ta₂O₅ dielectric, and the bottom electrode. Following the etch steps, individual capacitors were formed with dimensions of 0.8 × 0.8 mm, 0.9 × 0.9 mm, and 1.0 × 1.21 mm for the top plate, dielectric, and bottom plate, respectively. An optical microscope image of the capacitors is shown in Figure 4.3. At this stage, individual capacitors are ready for preliminary testing before integration of the TSVs.
4.3.2.2. Etching blind vias and filling with metal

Following testing of the fabricated capacitors, a 2 µm thick oxide was deposited by PECVD to protect the capacitors during TSV processing. The oxide was patterned and etched on both sides of the capacitors where TSVs were fabricated as shown in Figure 4.4.

To form the vias, a modified Bosch process was used that consisted of seven different modules with variable etch/passivation cycle times [37]. Varying the cycle time throughout the etch process provides the ability to control the shape of a via sidewall. A
via that exhibits tapering along the sidewall can be formed this way. The presence of a sidewall taper becomes critical when attempting to line via sidewalls with conformal thin films. Photolithography defined the via openings using AZ4330 photoresist. Vias were etched to a depth of approximately 100 µm. Vias that are not etched through the entire wafer are referred to as blind vias.

To insulate the vias, they were lined with a thin layer of oxide. A thin film of Ti was sputtered for the barrier layer and a thin film of Cu formed the seed layer for the electroplating step. The vias were filled with Cu by periodic pulse reverse plating. The filling process uses three successive plating steps as shown in Table 1. The steps are identified in the middle row as a, b, and c. A short DC plating step (step a) reinforces the seed layer [38]. A periodic waveform was used in plating steps b and c beginning with a forward current density of 4 mA/cm² (step b) that was increased to 8 mA/cm² (step c) once the aspect ratio becomes smaller. This technique allows filling vias without introduction of voids by adjusting the forward current density to the changing aspect ratio [37]. A value of 8 mA/cm² was used in the reverse direction for both steps b and c.

Plating times are shown for each step in the last row of Table 1.

| Reverse pulse waveform (ms) | 100 (Fwd)  
| 10 (Rev)  
| 100 (Off) |
| Current density (mA/cm²) | a) 4 (DC)  
| b) 4 (Fwd) & 8 (Rev)  
| c) 8 (Fwd) & 8 (Rev) |
| Plating time (min) | a) 1.5 (DC)  
| b) 120  
| c) 120 |
4.3.2.3. Front side patterning

During the via filling process, Cu builds up on the front side of the process wafer with increased thickness around the wafer edges. Because of this increased thickness, Cu was patterned and etched at the wafer edges, an area where no features are present. This etch is followed by another lithography step to pattern the area for etching the Cu between features. Defined contacts to capacitor plates were formed by patterning and etching oxide in a selected area. Front side processing ended with patterning and plating of Cu (M₃). M₃ refers to the connection between TSVs and capacitors (see Figure 4.4). At this point, the process wafer was bonded to a thick carrier wafer (650 µm) coated with 2 µm of thermally grown oxide.

4.3.2.4. Wafer attachment to a carrier wafer

The bonding process involved spin coating 16 µm of Brewer Science thermoplastic HT-10.10 on the carrier wafer. This material was baked in air at 160 °C for 3 min and the temperature was raised to 220 °C and baked for an additional 4 min. The process wafer was also baked at 110 °C for 2 min before stacking the wafers in a vacuum oven. The bonding temperature was set to 250 °C and the bonding process continued for approximately three hours with 13.2 lbs weights applied to the top of the stack. A PHI press was used to apply 2.5 tons of force at 225 °C to complete the bonding of process and carrier wafers. This wafer stack exhibited good planarity (±2 µm) over the entire stack and is a suitable value for the subsequent wafer thinning.
4.3.2.5. Wafer thinning

A Logitech lapping system was used to remove the bulk of silicon from the backside of the process wafer using an aluminum oxide (Al$_2$O$_3$) abrasive (grit size 15 µm) with the lapping plate rotating at 70 rpm. Alignment marks with large dimensions, and thereby etched deeper than the vias, were used to indicate when the user nears completion of the thinning process. At this stage, a smaller abrasive (grit size 9 µm) was used to begin repairing any damage induced in the silicon while approaching the via base. After bulk removal, a polishing step (grit size 0.3 µm) yielded a process wafer with a smooth and shiny backside.

4.3.2.6. Wafer backside processing

Following the thinning process, a lithography step was conducted to pattern and etch the remaining silicon and expose the via base using reactive ion etching (RIE). A PECVD oxide insulation layer was deposited followed by a patterning step used to etch oxide at the via base. Sputter deposition of Ti (barrier), Cu (seed), and Ti (to prevent Cu oxidation) followed the oxide etch. Another lithography step was used to pattern backside testing pads for DC electroplating of Cu, Ni, and Au following the Ti etch. The backside processing ends with a patterning step to etch Ti-Cu-Ti around the plated pads. Plating parameters used in forming the backside pads are shown in Table 4.2.
Table 4.2. Plating parameters used to form the backside testing pads.

<table>
<thead>
<tr>
<th>Electroplated Films</th>
<th>Cu</th>
<th>Ni</th>
<th>Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current density (mA/cm$^2$)</td>
<td>10</td>
<td>40</td>
<td>1.5</td>
</tr>
<tr>
<td>Plating time (min)</td>
<td>11</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Film thickness (µm)</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

4.4. Results and Discussion

In this study, the fabricated capacitors have an area of 0.81 mm$^2$ and a dielectric thickness of 200 nm. During TSV fabrication, temperatures as high as 250 °C were observed for some processing steps. The passive devices were tested before and after TSV fabrication. The intention of this series of tests was to assess capacitor performance after TSV processing. Leakage current was measured for different bias voltages. The device impedance as a function of frequency provided information about the frequency region where the device begins to behave like an inductor. Both capacitance and parasitic inductance measurements as a function of frequency are also useful measurements for determination of resonance frequency. In the following sections, capacitor testing results are described.

4.4.1. Leakage current as a function of bias voltage

Leakage currents are commonly observed to increase with increasing bias voltage and are mainly attributed to imperfections within the dielectric such as impurity centers and mechanical damage of the film [17]. In this study, leakage current was measured as a
function of bias voltage, before and after TSV processing, using an HP 4140B pA Meter/DC Voltage Source. The results are shown in Figure 4.5.

![Leakage current vs. bias voltage graph](image)

**Figure 4.5.** Leakage current as a function of bias voltage for capacitors before and after TSV processing.

The subsequent processing steps associated with TSV fabrication do not appear to contribute any serious negative effects on capacitor performance with respect to leakage current. When the bias voltage was less than 25 V, leakage currents did not exceed 5 µA. The leakage current increased with increasing bias voltages following the same trend regardless of exposure to TSV processing.

Because capacitors of this size are normally biased below 10 V, a small increase in leakage current due to integration with TSVs can be easily controlled. At a 10 V bias, the leakage currents for 120 capacitors were measured to be approximately 15 nA before integration of TSVs and 172 nA afterwards. Leakage current based on the capacitor operating voltage can be calculated using a selection limit of 10 nA/µFV, a value typically applied to solid tantalum electrolytic capacitors [39]. The idea of a selection
limit is used in industry to assess critical limits for leakage current values. Considering operation in our case at a 10 V bias voltage, the threshold for leakage current is 75.8 µA for an average capacitance of 758 pF. The measured leakage currents at a 10 V bias, following fabrication of TSVs, were two orders of magnitude lower than the selection limit. Leakage currents do not appear to be an issue when integrating capacitors with TSVs.

4.4.2. Leakage current as a function of time

Leakage current may increase over time and for this reason the measurement was repeated after the capacitor was maintained at the rated voltage for approximately 5 min. Leakage currents were measured for the capacitors every 30 sec over a time period of 6 min at different bias voltages both before and after TSV fabrication. The results are shown in Figure 4.6. While leakage current values increased after TSV processing, the final value was at an acceptable level. Leakage currents were approximately 1 µA for a bias voltage as high as 15 V after TSV processing. As a general trend, a decrease in leakage current of approximately 20 % over time was observed over the entire range of bias voltages. An explanation for this trend is considered to be due to three components [39]. These components include: the charging current \( \log I = A - Bt \), a value that is negligible after a few seconds; a current that is inversely proportional to time \( I*\rho = \text{constant} \); and a current changing only slowly with time. Overall, the combination of these parameters leads to a reduction in leakage current over time as observed in this study.
The process flow for fabricating TSVs requires some of the processing steps to reach temperatures as high as 250 °C. Due to this temperature exposure, capacitor leakage current was observed to increase when compared to measured values before TSV fabrication. This increase is believed to be due to impurities generated within the Ta$_2$O$_5$ dielectric following oxygen diffusion as explained by Smyth et al. [21]. This phenomenon may be suppressed by using a barrier layer in order to prevent oxygen diffusion and preserve the quality of the Ta$_2$O$_5$ dielectric following TSV processing. As stated earlier, for capacitors of this size that operate at bias voltages no larger than 10 V, the measured leakage currents were well within acceptable limits following TSV processing. For this reason we did not consider adding a barrier layer in the fabrication of capacitors although this layer is essential in preventing oxygen diffusion.
4.4.3. Impedance response as a function of frequency

Impedance measurements were obtained using an HP 4291A RF Impedance/Material Analyzer over a frequency range of 1 MHz to 1.8 GHz. This equipment measures impedance by applying a stimulus signal to the capacitor while measuring the complex voltage and complex current. Impedance is derived from this measurement and an equivalent series circuit is modeled from which the R, L, and C parameters are calculated. The inductance and resistance in the model are called equivalent series inductance (ESL) and equivalent series resistance (ESR). ESR comes primarily from the top and bottom plate materials of the capacitor where the ESL is a product of the plate geometry.

Impedance measurements as a function of frequency are very important for capacitors as the components constituting the device impedance change with the applied signal frequency. Therefore, impedance plots must be studied for the frequency range of operation for the capacitor. From this series model, the impedance at a particular frequency is given by:

\[ Z = \sqrt{R^2 + (X_L - X_C)^2} \]  \hspace{1cm} (3)

where \( X_L = 2\pi f L \)  \hspace{1cm} (4)
defines the inductor’s opposition to current flow and

\[ X_C = \frac{1}{2\pi f C} \]  \hspace{1cm} (5)
defines the capacitor’s opposition to current flow. The impedance values obtained represent the overall resistance to alternating current (AC) flow offered by these three
components. At resonant frequency, \( X_C \) and \( X_L \) are equal to each other and only the resistance component exists. As shown in Figure 4.7, the average resonant frequency for our capacitors was 683 MHz with a standard deviation of 1.4 % before TSV processing and 560 MHz with a standard deviation of 0.8 % after TSV processing. Therefore, the fabricated capacitors have capacitive behavior at frequencies below 560 MHz and inductive behavior beyond the resonant frequency value. This behavior is explained by equations (4) and (5) where at low frequencies, \( X_C \) dominates the reactance component of the impedance before \( X_L \) dominates at higher frequencies. Detailed behavior of each of these components that contribute to the overall impedance is given in the following section.

![Graph showing impedance as a function of frequency before and after TSV processing.](image)

**Figure 4.7.** Impedance as a function of frequency before and after TSV processing.

### 4.4.4. Capacitance, inductance, and resistance as a function of frequency

The performance of the capacitors, for applications such as high speed decoupling capacitors, was evaluated by measuring resonant frequency, parasitic inductance, and
parasitic resistance. Measurements for the same capacitors, before and after TSV processing, allowed a direct comparison of the device parameters showing the impact of fabricating TSVs following capacitor fabrication. Capacitance and ESL as a function of frequency is shown in Figure 4.8.

![Capacitance and inductance measurements as a function of frequency before and after TSV processing.](image)

Figure 4.8. Capacitance and inductance measurements as a function of frequency before and after TSV processing.

The capacitance appears to be stable with regard to frequency as evidenced by average values very close to 683 pF with a standard deviation of only 0.2 % for the frequency range studied (1 MHz - 1.8 GHz). This average capacitance value represents a density of 107 nF/cm². Increasing capacitor density is a focus of current research for applications involving continuously shrinking electronics assemblies. Previous studies showed that 100 nF/cm² was achieved with a 200 nm Ta₂O₅ dielectric [14]. The density obtained in our study can be further increased by reducing the dielectric thickness if high leakage currents are not an issue. Multilayer capacitors were proven to double or triple the capacitance density obtained with a single layer. Thomason et al. obtained a
capacitance density of 220 nF/cm² using a standard 2-layer 200 nm thick dielectric [15].
The density obtained was doubled by reducing the dielectric thickness to 100 nm on both
layers [15]. To further increase the density, Schaper et al. used a triple-layer process with
a 100 nm thick dielectric yielding a capacitor density of 600 nF/cm² [16]. However, that
process was expensive and resulted in low yields making it unsuitable for large-scale
production. In our studies, measured capacitance was found to increase following TSV
processing and is believed to be due to oxygen diffusion from the Ta₂O₅ dielectric film.
An average capacitance value of 758 pF with a standard deviation of 0.9 % was observed
over the measured frequency range. This increase was due to the reduction in dielectric
thickness. This observation is consistent with results observed by Smyth et al. showing
that capacitance has a strong frequency and temperature dependence [21].

The parasitic inductance of the capacitors over the range of frequencies studied
had an average value of 80 pH with a standard deviation of 2.9 %. Inductance as a
function of frequency is shown in Figure 4.8. Following the processing of TSVs at some
temperatures as high as 250 °C, the parasitic inductance increased to an average value of
107 pH with a standard deviation of 2.2 %.

The parasitic resistance followed the same trend observed for parasitic inductance
with average values increasing from 155 mΩ to 240 mΩ following TSV processing as
shown in Figure 4.9. The ESR appears to be unstable over the measured frequency range
with a standard deviation of 14.2 % observed before TSV integration. Annealing that
potentially occurs during TSV processing may have led to an increased stability with a
standard deviation of only 5.0 %. Kim et al. performed similar studies and measured
approximately 150-250 mΩ for their series model [11]. Their studies revealed that the
omission of the ESR in the electrical model gives unrealistic results for the frequency response of the Ta$_2$O$_5$ films. In their model, they accounted for the observed self-resonance beyond 3 GHz by adding a series impedance and a parallel resistance [11].

Figure 4.9. Resistance measurements as a function of frequency before and after TSV processing.

4.5. Conclusions

In this study, capacitors using Ta$_2$O$_5$ as the dielectric were integrated with TSVs in order to observe the effects of TSV processing on the performance of the capacitors. Ta$_2$O$_5$ dielectric films prepared by anodization of sputtered tantalum (Ta) were found to exhibit satisfactory electrical properties. At a 10 V bias, the leakage currents for 120 capacitors were measured to be approximately 15 nA before integration of TSVs and 172 nA afterwards with some processing temperatures as high as 250 °C. The performance of the capacitors, for applications such as high speed decoupling capacitors, was also evaluated by measuring resonant frequency, parasitic inductance, and parasitic resistance.
The capacitance of fabricated capacitors appears to be stable with regard to frequency as evidenced by average values very close to 683 pF with only 0.2 % standard deviation in the range of frequencies studied (1 MHz - 1.8 GHz). The average resonant frequency for these capacitors was found to be 683 MHz with a standard deviation of 1.4 % before TSV processing and 560 MHz with a standard deviation of 0.8 % after TSV processing. Overall, TSV processing was found to have minor effects on the performance of fabricated capacitors.

Acknowledgements

This work is supported by the College of Engineering and the Central Analytical Facility at the University of Alabama. The assistance of the technical staff of the High Density Electronics Center at the University of Arkansas is also acknowledged.

4.6. Chapter 4 References


CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

TSV technology allows devices to be connected in a three-dimensional manner. Some advantages of this technology include lower power dissipation, reduction of timing delays, and increased integration density resulting in improved electrical performance. Fabrication of robust TSVs is critical for any system integration process.

In this research project, TSVs were fabricated and tested with dimensions of approximately 45 μm in diameter and depths of 95 μm. Resistance was measured for single vias and various via chains. The vias were found to be well insulated from each other. Yields were in the range of 99.93%. Vias were further investigated for reliability through temperature cycling with temperatures ranging from -25 °C to 125 °C. Wire bonds were found to be the source of increasing resistance during thermal cycling so the cycling was performed with a different approach that involved wire bonding only immediately before and after the test. When 200 cycles were conducted, small changes in via chain resistance were observed with preservation of via chain continuity. A resistance value change in the range of 7.2% was observed in via chains after 1000 cycles in a test performed at the Missouri University of Science and Technology. Investigation of the discontinuity observed between two vias revealed, through repeated sample polishing and imaging, that this problem was a surface defect. The vias under study appeared to be stable to temperature cycling. Similar stability results were obtained following storage of
vias at temperatures as high as 250 °C for 200 hrs with no large increase in resistance measured.

The significant mismatch in the coefficients of thermal expansion (CTE) of silicon (2.6 ppm/°C), copper (16.5 ppm/°C), and dielectric materials such as silicon dioxide (0.4 ppm/°C) is a source of thermomechanical stress accumulation at the interface of these materials. This stress is the main cause for crack formation and dielectric delamination at an interface when stress at the interfaces exceeds their adhesion strength. This may cause reliability problems that result in electrical breakdown. The extent of stress distribution around the copper via strongly depends on the via dimensions and profile. Although tungsten has a CTE more similar to silicon and is commonly used in IC fabrication processes, the maximum achievable film thickness is limited to a few microns. Since it is a refractory material, it is difficult to lower the stress by annealing. For these reasons, more interest has been given to TSVs filled with highly conductive copper. Heating a silicon device with copper TSVs causes high compressive stresses in the copper that expands to release the stress. An IMEC research team has found that a short anneal before CMP will stabilize the copper into a low-stress condition upon subsequent thermal steps [1].

In order to increase the via etch rate and eliminate the scalloping typically observed from the Bosch process, vias were etched at cryogenic temperatures. The vias formed by ICP cryogenic etching had a tapered sidewall due to control of process parameters. Substrate temperature and the percentage of oxygen in the gas mixture were found to be key parameters affecting the via sidewall angle. A tapered via profile with an 87º angle was obtained using a substrate temperature of -90 °C and 14 % oxygen in the
SF₆/O₂ mixture. With the resulting process recipe, silicon grass was found to be substantially reduced for our feature sizes. Silicon grass is a problem in many etch processes and can be particularly problematic in cryogenic etching. Etch rates as high as 4 μm/min, for a 35 minute etch, were reached through careful selection of process parameters. Positive photoresist, thicker than 1.3 μm, was found to be more prone to cracking at cryogenic temperatures necessitating a hard mask for deep etching. From the three hard mask materials studied, Al yielded a large density of silicon spikes due to micromasking; a Cr mask generated bowing at the top of the via; and a SiO₂ mask provided the best overall profile. This mask material was used to produce tapered via sidewalls. The silicon etch rate was found to increase with pressure in a chemical-limited reaction regime up to a chamber pressures of 20 mTorr where the highest etch rate was observed before decreasing in a physical-limited reaction regime beyond this pressure. As chamber pressure was increased, it becomes more and more difficult to control the via profile. Finally, mask selectivity decreases with an increase in ICP power and increases with chamber pressure up to a value of 20 mTorr.

To illustrate the advantages of TSV technology, a simple integration test vehicle was created. Capacitors using Ta₂O₅ as the dielectric were integrated with TSVs in order to observe the effects of TSV processing on the performance of the capacitors. Ta₂O₅ dielectric films prepared by anodization of sputtered tantalum (Ta) were found to exhibit satisfactory electrical properties. The performance of the capacitors, for applications such as high speed decoupling capacitors, was also evaluated by measuring resonant frequency, parasitic inductance, and parasitic resistance. The capacitance appears to be more stable in the range of frequencies studied (1 MHz-1.8 GHz). The resonant
frequency was found to be 683 MHz with a standard deviation of 1.4 % before TSV processing and decreased to 560 MHz with a standard deviation of 0.8 % after TSV processing. This shift in electrical properties was expected due to the temperatures the capacitors were exposed to during TSV processing. Overall, TSV processing was found to have minor effects on the capacitor performance and this was encouraging for future integration efforts.

5.2. Future Work

TSV fabrication, testing, and developing an integration prototype were the focus of this work. Reliability data has been presented that complements the existing research published on TSV technology. This dissertation represents improvement of the existing knowledge and provides insight for future development. In advanced packaging applications, decoupling capacitors are used to supply the instantaneous current needed for switching while minimizing switching noise. Increasing significantly the density of these capacitors can be achieved using TSV technology and allowing these capacitors to be fabricated in close proximity to the active elements. Therefore, higher clock rates could be obtained by reducing their parasitic inductance. This dissertation research shows the feasibility of achieving the goal of integration without compromising the operation of these devices. However, capacitance density values obtained in this study would be significantly improved by using a multilayer capacitor with a reduced dielectric thickness. This process would also improve or increase the resonant frequency observed in this work. Defect density and leakage currents would be reduced by using a TaN barrier layer to prevent oxygen diffusion from the dielectric film at higher temperatures.
5.3. Chapter 5 Reference

APPENDICES
APPENDIX A

JOURNAL/CONFERENCE CONTRIBUTIONS

JOURNAL CONTRIBUTIONS


CONFERENCE CONTRIBUTIONS


APPENDIX B

PROCESS STEPS FOR THE INTEGRATION OF CAPACITORS USING TSVs

Fabricated capacitors  Protection of capacitors with oxide

Oxide patterning around capacitors  TSV patterning around capacitors
Etched TSVs around capacitors

Thick Cu patterning

Thick Cu etched

Patterning of contact through oxide for connection with TSVs
Contact etched through oxide

Alignment mark used for the patterning process

Metal 3 connection patterning

Metal 3 plated for connection of TSVs with top and bottom plates
Backside patterning for Si etch and via base exposure

Alignment mark used for RIE patterning

Backside oxide patterning

Backside oxide etched
Patterning backside pad for electroplating of Cu, Ni, and Au

Electroplated Au on the backside TSV testing pad

Background seed patterning

Background seed etched
Alignment mark used for patterning and plating backside testing pad

Alignment mark used for patterning background seed
APPENDIX C

SOME OF THE TOOLS USED FOR EXPERIMENTS

C1. Surface Technology Systems Advanced Silicon Etcher (ASE-Gen1)
C2. Plasma Therm SLR720 Reactive Ion Etch tool
C3. Oxford Instruments Plasma Lab 100 used for etching at cryogenic temperatures
C4. Plasma-Therm SLR730 load-locked, parallel plate PECVD tool
C5. Varian XM-8 Sputtering system
C6. Copper plating system
C7. Eaton 6000 2-track cassette-to-cassette coater with bake system
C8. Karl Suss MA150 Aligner
C.9. JEOL JSM-7000F Field Emission Scanning Electron Microscope
C10. Bonding with the PHI hydraulic press
C11. Logitech PM5 Lapping system
C12. Quantum Design Physical Property Measurement System
C13. YES HMDS oven

C14. APE-110 Oxygen Plasma Asher
C15. Dektak profilometer

C16. Bonding in a Fisher Isotemp vacuum oven Model-282
C17. Roto Pol-22 used for sample polishing
# APPENDIX D

## PROCESS TRAVELER FOR TSV FABRICATION

<table>
<thead>
<tr>
<th>PROCESS STEPS</th>
<th>PROCESS ENGINEER NOTES</th>
<th>PROCESS PARAMETERS</th>
<th>EQUIPMENT</th>
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</thead>
<tbody>
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<td></td>
<td><strong>DESCRIPTION</strong></td>
<td><strong>PWR</strong></td>
<td><strong>INTENSITY</strong></td>
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<td><strong>Wafer (5&quot;)Cleaning</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 SRD</td>
<td>Remove particles</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 HMDS</td>
<td>Plasma with the parameters or spin-on and 2 min bake</td>
<td>150°C, 8mTorr</td>
<td>150°C, 8mTorr</td>
</tr>
<tr>
<td><strong>Via Patterning (ViaTop Mask)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Apply Resist</td>
<td>Recipe #1, Positive AZ-4330</td>
<td>3min @110°C</td>
<td>320 mJ</td>
</tr>
<tr>
<td>2 Expose</td>
<td>Exposure Time = Energy / Intensity</td>
<td>8 µm</td>
<td>8 µm</td>
</tr>
<tr>
<td>3 Develop</td>
<td>AZ400K (3:1)</td>
<td>2 min</td>
<td>2 min</td>
</tr>
<tr>
<td>4 DR / SRD</td>
<td>Dump Rinse / Spin Rinse Dry</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 Inspection</td>
<td>Clean patterning, open and no resist</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 Hard Bake</td>
<td>Improve PR hardness and adhesion</td>
<td>110°C</td>
<td>110°C</td>
</tr>
<tr>
<td>7 Measure</td>
<td>Measure resist thickness</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>STS Chamber Cleaning (Use Si wafer with oxide (2 um) on it for cleaning)</strong> Note: Do cleaning after processing 3 wafers.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Chamber Cleaning</td>
<td>Program: 02 CLEAN</td>
<td>30 W</td>
<td>30 W</td>
</tr>
<tr>
<td></td>
<td>O2: 49 sccm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Platen Power(W)=30/0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Coil Power(W)= 800/800 APC=78</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>STS Chamber Conditioning (Use Bare Silicon wafer)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Chamber Conditioning</td>
<td>Program: ETCH_30</td>
<td>30 W</td>
<td>30 W</td>
</tr>
<tr>
<td></td>
<td>SF6: 49 sccm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Platen Power(W)=20/0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Coil Power(W)= 700/700 APC=50°</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Via Etching by DRIE

<table>
<thead>
<tr>
<th></th>
<th>Program: AK 83AR2</th>
<th>30 W</th>
<th>2 hr 40 min</th>
<th>STS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DRIE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SF6: 112 sccm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C4F8: 85 sccm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Platen Power(W)=12/0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Coil Power(W)=200/200</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>APC= 60°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Profile with via sidewall angle of 83 degree and AR 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>No of Modules= 7, No. of Cycles =37</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: C4F8 flow rate is different in Mod 1 &amp; 2, APC = 50° for Mod 1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Measure resist thickness</th>
<th></th>
<th>Nanospec</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Descum</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Remove remaining PR</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Concentrated Sulfuric Acid + Hydrogen Peroxide 30% 3:1</td>
<td>20 + 20 min</td>
<td>Piranha</td>
</tr>
</tbody>
</table>

### SiO2 Deposition (Insulation Layer)

<table>
<thead>
<tr>
<th></th>
<th>Deposit 2um oxide</th>
<th>250°C</th>
<th>2 um</th>
<th>22 min</th>
<th>PECVD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Check Oxide Thickness</td>
<td>Record Actual Oxide Thickness</td>
<td></td>
<td></td>
<td>Nanospec</td>
</tr>
</tbody>
</table>

### Ti (Diffusion Barrier) + Cu (Seed)

<table>
<thead>
<tr>
<th></th>
<th>RF SPUTTER WAFERS</th>
<th>RF Etch</th>
<th>60 sec</th>
<th>XM8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SPUTTER Ti</td>
<td>(8 passes)</td>
<td>2500 W</td>
<td>0.5 um</td>
</tr>
<tr>
<td>9</td>
<td>SPUTTER COPPER</td>
<td>(15 passes)</td>
<td>3000 W</td>
<td>5 um</td>
</tr>
</tbody>
</table>
### Copper Plating

<table>
<thead>
<tr>
<th>Step</th>
<th>Task Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Set up bath</td>
<td>Check plating bath level</td>
</tr>
<tr>
<td>2</td>
<td>Condition Anode</td>
<td>Heat Cu Etchant (APS 100) to 30°C, Clean Anode Thorougly, Wet Etch (10% H₂SO₄ soln)</td>
</tr>
<tr>
<td>3</td>
<td>Cu test plate (using Hull Cell)</td>
<td>Place in Plating Bath and Use dummy wafer to condition the anode, USE Program #1, Leave anode in the plating bath for 10 min</td>
</tr>
<tr>
<td>4</td>
<td>Supply organic Additives</td>
<td>Check organic levels, Protect Alignment marks with blue tape</td>
</tr>
<tr>
<td>5</td>
<td>Set Plating Profile</td>
<td>Program Setup, Cu Bath SC MD:8 ml/l of solution supply, 0.8 ml/Ah, Cu Bath SC LO 70/30:2 ml/l, 0.2 ml/Ah</td>
</tr>
</tbody>
</table>

### Front Contact Patterning (MTop Mask)

<table>
<thead>
<tr>
<th>Step</th>
<th>Task Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Apply Resist and Soft bake</td>
<td>Recipe #1, Positive AZ-4330</td>
</tr>
<tr>
<td>2</td>
<td>Expose</td>
<td>Use Mask: MTOP, 3 min @110°C, 8 µm</td>
</tr>
<tr>
<td>3</td>
<td>Develop</td>
<td>AZ400K (3:1), 320 mJ</td>
</tr>
<tr>
<td>4</td>
<td>DR / SRD</td>
<td>Dump Rinse / Spin Rinse Dry</td>
</tr>
<tr>
<td>5</td>
<td>Inspection</td>
<td>Clean patterning, open and no resist</td>
</tr>
<tr>
<td>6</td>
<td>Hard Bake</td>
<td>2 min Hot plate</td>
</tr>
<tr>
<td>7</td>
<td>Measure</td>
<td>Measure resist thickness</td>
</tr>
</tbody>
</table>

Notes:
1) Use a clear mask to locate alignment before using the actual MTOP mask
2) Use the cross (+) alignment mark for aligning.
<table>
<thead>
<tr>
<th><strong>Cu Etch</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Cu Etch</td>
<td>Heat 40C, APS 100, Etch until TaN visible</td>
<td></td>
<td></td>
<td>About 10 min</td>
</tr>
<tr>
<td>2</td>
<td>Hard Bake</td>
<td></td>
<td></td>
<td></td>
<td>2 min Hot plate</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Ti Etch</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ti Etch</td>
<td>Use 1FABCLN recipe to clean system</td>
<td></td>
<td></td>
<td>20 sec</td>
</tr>
<tr>
<td>2</td>
<td>Conditioning</td>
<td>RIE etch: Program name: ISI Use Ti wafer as substrate</td>
<td></td>
<td></td>
<td>15 min</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>TaN etch</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TaN</td>
<td>RIE etch: Program name: ISI O2 =7sccm , SF6 =70sccm , Ar =30sccm, Pressure=200mTorr, Power =100W (1) Place Al wafer first on the chuck before putting your wafer. For easy distribution of heat while etching (2) Make sure oxide is visible after etch</td>
<td></td>
<td></td>
<td>6 min</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>PR Removal</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Expose resist 3X the exposure time using blank mask</td>
<td></td>
<td></td>
<td></td>
<td>320 mJ</td>
</tr>
<tr>
<td>2</td>
<td>Develop</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Remove remaining resist in AZ300T bath</td>
<td></td>
<td></td>
<td></td>
<td>10 min</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Process Wafer Attachment Using LCP</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Initial Thickness</td>
<td>Process Wafer</td>
<td></td>
<td></td>
<td>380um Pressure Plates</td>
</tr>
<tr>
<td>2</td>
<td>Thickness</td>
<td>Process wafer after plating</td>
<td></td>
<td></td>
<td>395 um</td>
</tr>
<tr>
<td>3</td>
<td>Thickness</td>
<td>Carrier wafer</td>
<td></td>
<td></td>
<td>625 um</td>
</tr>
<tr>
<td>4</td>
<td>Thickness</td>
<td>Wafer Stack</td>
<td></td>
<td></td>
<td>1064 um</td>
</tr>
<tr>
<td>5</td>
<td>Planarity</td>
<td>Wafer Stack</td>
<td></td>
<td></td>
<td>±2 um</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Wafer Grinding</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Planarity</td>
<td>Of the lapping plate</td>
<td></td>
<td></td>
<td>0 Logitech</td>
</tr>
<tr>
<td>2</td>
<td>Abrasive</td>
<td>Grit size of the abrasive</td>
<td></td>
<td></td>
<td>15 um</td>
</tr>
<tr>
<td>3</td>
<td>RPM</td>
<td>Lapping plate RPM</td>
<td></td>
<td></td>
<td>70 RPM</td>
</tr>
<tr>
<td>4</td>
<td>Lapping Time</td>
<td>Time wafer backgrinded</td>
<td></td>
<td></td>
<td>75 min</td>
</tr>
<tr>
<td>5</td>
<td>Thickness</td>
<td>Thickness of backgrinded wafer stack</td>
<td></td>
<td></td>
<td>809 um</td>
</tr>
<tr>
<td>6</td>
<td>Planarity</td>
<td>Variance in thickness of wafer stack</td>
<td></td>
<td></td>
<td>±5</td>
</tr>
</tbody>
</table>
### Wafer Polishing

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Polishing plate</td>
<td></td>
<td>Logitech</td>
</tr>
<tr>
<td>2</td>
<td>Abrasive</td>
<td>Grit size of the abrasive</td>
<td>0.3 um</td>
</tr>
<tr>
<td>3</td>
<td>RPM</td>
<td>Lapping plate RPM</td>
<td>45 RPM</td>
</tr>
<tr>
<td>4</td>
<td>Time</td>
<td>Polishing Time</td>
<td>45 min</td>
</tr>
<tr>
<td>5</td>
<td>Thickness</td>
<td>Thickness of polished wafer</td>
<td>805 um</td>
</tr>
<tr>
<td>6</td>
<td>Planarity</td>
<td>Variance in thickness of wafer stack</td>
<td>±5</td>
</tr>
</tbody>
</table>

### Backside Patterning (SiEtch Mask)

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Inspect using Microscope</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Quick Cu ETCH (If necessary)</td>
<td>20 sec</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Inspect using Microscope</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>HMDS</td>
<td>Spin on HMDS</td>
<td>Using recipe #7</td>
</tr>
<tr>
<td>5</td>
<td>Apply Resist</td>
<td>Recipe #3, Positive AZ-4330</td>
<td>6 min @110°C</td>
</tr>
<tr>
<td>6</td>
<td>Expose</td>
<td>Use Mask: SiEtch, Use Short Program</td>
<td>8 μm</td>
</tr>
<tr>
<td>7</td>
<td>Develop</td>
<td>AZ400K (3:1)</td>
<td>Notes: (1) Use a clear mask to locate alignment before using the actual SiEtch mask</td>
</tr>
<tr>
<td>8</td>
<td>Inspection</td>
<td>Clean patterning, open and no resist</td>
<td>Although, the resist is 8 um thick, the exposure energy, exposure and bake time has to be increase to take into account the new thickness of the wafer. Note, a carrier has been attached to process wafer</td>
</tr>
<tr>
<td>9</td>
<td>Hard Bake</td>
<td>Improve PR hardness and adhesion</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Measure</td>
<td>Measure resist thickness</td>
<td>(2) Use circle features for alignment</td>
</tr>
</tbody>
</table>

### RIE Etch

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RIE</td>
<td>Program: Zia</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Time</td>
<td>Etch until Copper Post visible. Use DekTek to measure the depth.</td>
<td>SF6: 40 sccm O2: 15 sccm DC: 100 V P: 100 mTorr</td>
</tr>
</tbody>
</table>

### PR Removal

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Expose resist 3X the exposure time using blank mask</td>
<td>320 mJ</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Develop</td>
<td></td>
<td>10 min</td>
</tr>
<tr>
<td>3</td>
<td>Remove remaining resist in AZ300T bath</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### SiO2 Deposition (Insulation Layer)

<table>
<thead>
<tr>
<th>Step</th>
<th>Task</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Deposit oxide</td>
<td>Also deposit oxide on dummy wafer to check for SiO2 etch rate</td>
</tr>
<tr>
<td>2</td>
<td>Check Oxide Thickness</td>
<td>Record Actual Oxide Thickness</td>
</tr>
</tbody>
</table>

- **Temperature**: 325°C  
- **Thickness**: 2 µm  
- **Time**: 22 min  
- **Process**: PECVD  
- **Equipment**: Nanospec

### SiO2 Etch Patterning (SiO2 Etch Mask)

<table>
<thead>
<tr>
<th>Step</th>
<th>Task</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HMDS</td>
<td>Spin on HMDS</td>
</tr>
<tr>
<td>2</td>
<td>Apply Resist</td>
<td>Recipe #3, Positive AZ-4330</td>
</tr>
<tr>
<td>3</td>
<td>Develop</td>
<td>Expose using SiO2 Etch mask</td>
</tr>
<tr>
<td>4</td>
<td>DR / SRD</td>
<td>Develop photoresist, Dump &amp; Rinse</td>
</tr>
<tr>
<td>5</td>
<td>Inspection</td>
<td>Inspect using Microscope</td>
</tr>
<tr>
<td>6</td>
<td>Measure</td>
<td>Measure resist thickness</td>
</tr>
</tbody>
</table>

- **Exposure**: 2 min \(\text{at } 110°C\)  
- **Thickness**: 4.5 µm  
- **Time**: 2 min  
- **Equipment**: Suss 275  
- **Measurements**: Microscope, Nanospec

### Wet Etch SiO2

<table>
<thead>
<tr>
<th>Step</th>
<th>Task</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Check solution level</td>
<td>Add water if low</td>
</tr>
<tr>
<td>2</td>
<td>Start Bubbler</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Press Heat On</td>
<td>Use the dummy wafer to check the approximate etch rate before etching actual sample</td>
</tr>
<tr>
<td>4</td>
<td>Wait till solution reach temp of 40 C</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Dip water carrier in the bath</td>
<td></td>
</tr>
</tbody>
</table>

**PR Removal**

<table>
<thead>
<tr>
<th>Step</th>
<th>Task</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Expose resist 3X the exposure time using blank mask</td>
<td>320 mJ</td>
</tr>
<tr>
<td>2</td>
<td>Develop</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Remove remaining resist in AZ300T bath</td>
<td>10 min</td>
</tr>
</tbody>
</table>

### Ti/Cu/Ti Seed Layer Deposition (Diffusion Barrier)

<table>
<thead>
<tr>
<th>Step</th>
<th>Task</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SPUTTER Ti</td>
<td>1 pass of Ti</td>
</tr>
<tr>
<td>2</td>
<td>SPUTTER COPPER</td>
<td>1 pass of Cu</td>
</tr>
<tr>
<td>3</td>
<td>SPUTTER Ti</td>
<td>1 pass of Ti</td>
</tr>
</tbody>
</table>

- **Power**: 1700 W  
- **Time**: 11 sec  
- **Equipment**: XM8
### Backside Patterning MBot Mask

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Recipe/Parameters</th>
<th>Temperature</th>
<th>Time</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Apply Resist</td>
<td>Recipe #3, Positive AZ-4330</td>
<td></td>
<td></td>
<td>2 min @ 110°C</td>
</tr>
<tr>
<td>2</td>
<td>Expose</td>
<td>Use Mask: Mbot</td>
<td></td>
<td>160 mJ</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Develop</td>
<td>AZ400K (3:1)</td>
<td></td>
<td>1:30 min</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Inspection</td>
<td>Clean patterning, open and no resist</td>
<td></td>
<td></td>
<td>Microscope</td>
</tr>
<tr>
<td>5</td>
<td>Measure</td>
<td>Measure resist thickness</td>
<td></td>
<td></td>
<td>Nanospec</td>
</tr>
<tr>
<td>6</td>
<td>Harb Bake</td>
<td></td>
<td></td>
<td>2 min @ 110°C</td>
<td></td>
</tr>
</tbody>
</table>

### Copper Plating

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ti Etch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Supply organic Additives</td>
<td>Check organic levels</td>
<td>Determine Organic additive addition levels</td>
<td>8L Plating Bath</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Set Plating Profile</td>
<td>8.4 cm²</td>
<td>4 µm</td>
<td>ON (100 ms) Current (0.084 A)</td>
<td>Off (0 ms) Current (0.084 A)</td>
<td>Rev (10 ms) Duration (0.019Ahr)</td>
</tr>
</tbody>
</table>

### PR Removal

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Expose resist 3X the exposure time using blank mask</td>
<td></td>
<td>160 mJ</td>
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<tr>
<td>2</td>
<td>Develop</td>
<td></td>
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</tr>
<tr>
<td>3</td>
<td>Remove remaining resist in AZ300T bath</td>
<td></td>
<td>10 min</td>
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</tbody>
</table>

### Cu seed Background etch (MBSEED Mask)

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Recipe/Parameters</th>
<th>Temperature</th>
<th>Time</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Apply Resist</td>
<td>Recipe #3, Positive AZ-4330</td>
<td></td>
<td></td>
<td>3 min @ 110°C</td>
</tr>
<tr>
<td>2</td>
<td>Expose</td>
<td>Use Mask: Mbot</td>
<td></td>
<td>320 mJ</td>
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</tr>
<tr>
<td>3</td>
<td>Develop</td>
<td>AZ400K (3:1)</td>
<td></td>
<td>1:30 min</td>
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</tr>
<tr>
<td>4</td>
<td>Inspection</td>
<td>Clean patterning, open and no resist</td>
<td></td>
<td></td>
<td>Microscope</td>
</tr>
<tr>
<td>5</td>
<td>Measure</td>
<td>Measure resist thickness</td>
<td></td>
<td></td>
<td>Nanospec</td>
</tr>
<tr>
<td>Etch Ti, Cu and Ti</td>
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<td>-------------------</td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>Ti Etch</td>
<td>Ti wet etch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Cu Etch</td>
<td>Heat 40C, Check etch rate on the bottle</td>
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</tr>
<tr>
<td>1</td>
<td>Ti Etch</td>
<td>Ti wet etch</td>
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<table>
<thead>
<tr>
<th>PR Removal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
</tbody>
</table>

| Electrical Testing |